

# **Appendix E7**

## ***Logic Family Signal Integrity Comparisons***

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11/10/99

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\* Indicates an unfinished section

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## Signal Integrity (SI) Summary and Recommendations

Only some very general recommendations are made regarding the choice of a default IBIS model for different logic levels. The recommendation of a particular technology as "best" for a particular application is not made.

This catalog of SI response was originally put together to aid in choosing a default IBIS model for each of the major logic family classifications into voltage ranges. Cadence Design Systems, Inc., SI simulation tools are used here at 3Com and they come set up with a 5 volt default IBIS model, CDSDefault - - -. Similarity to that model is used to guide my choices in other voltage ranges. The semiconductor industry's major voltage ranges appear to be 5, 3.3, 2.5-2.1 and (possibly in the future) 1.8-1.5. These voltages refer to the Vcc supply voltage and do not consistently imply a set value for the switching threshold standards of Vol, Vil, Vt, Vih, and Vol once you choose the Vcc. Further, backplane and differential switching are really categories by themselves.

Default choices are merely a starting point for running SI simulations when you do not have an IBIS model for the part. They are set up because, for instance, 2.1 volt logic has switching threshold standards that are totally inconsistent with 5 volt logic parts. Thus, totally irrelevant reports on noise margin, indeed the ability to switch at all, will result by letting the simulator automatically fall through to CDSDefault in all cases.

|                  |            |
|------------------|------------|
| 5.0 volt choice: | CDSDefault |
| 3.3 volt choice: | LVT        |
| 2.5 volt choice: | ALB        |

2.1 (and below) volt choices: Not enough data as of this date: 9/22/99.

|                    |                  |
|--------------------|------------------|
| Backplanes:        | LVT <sup>1</sup> |
| Differential nets: | LVT <sup>2</sup> |

Defaults are only good for seeing if a net is functional at all. As topology becomes more complex and frequency (edge rate) goes up they become less relevant even as a first approximation.

This report will be updated as more IBIS models become available.

---

<sup>1</sup> LVT has reasonable capability to run on a bi-directional unterminated daisy-chain bus. GTLP actually performs much better than LVT, but is more expensive. For large, complex busses switch to GTLP.

<sup>2</sup> By default, at this point in time.

## Switching Standards

| Family | Vol | Vil | Vt  | Vih | Voh  | Vcc |
|--------|-----|-----|-----|-----|------|-----|
| ABT    | .4  | .8  | 1.5 | 2.0 | 2.4  | 5   |
| ABTE   | .4  | 1.4 | 1.5 | 1.6 | 2.4  | 5   |
| AC     | .5  | 1.5 | 2.5 | 3.5 | 4.44 | 5   |
| ACQ    |     |     |     |     |      | 5   |
| ACT    | .4  | .8  | 1.5 | 2.0 | 2.4  | 5   |
| ACTQ   |     |     |     |     |      | 5   |
| AHC    | .5  | 1.5 | 2.5 | 3.5 | 4.44 | 5   |
| AHCT   | .4  | .8  | 1.5 | 2.0 | 2.4  | 5   |
| AS     |     |     |     |     |      | 5   |
| ALS    |     |     |     |     |      | 5   |
| FAST   |     |     |     |     |      | 5   |
| HC     | .5  | 1.5 | 2.5 | 3.5 | 4.44 | 5   |
| HCT    | .4  | .8  | 1.5 | 2.0 | 2.4  | 5   |
| LS     |     |     |     |     |      | 5   |
| S      |     |     |     |     |      | 5   |
| TTL    |     |     |     |     |      | 5   |
| VHC    |     |     |     |     |      | 5   |
| VHCT   |     |     |     |     |      | 5   |
|        |     |     |     |     |      |     |
| AC     |     |     |     |     |      | 3.3 |
| ACQ    |     |     |     |     |      | 3.3 |
| ALVC   | .4  | .8  | 1.5 | 2.0 | 2.4  | 3.3 |
| ALVT   | .4  | .8  | 1.5 | 2.0 | 2.4  | 3.3 |
| HSTL   | .4  | .65 | .75 | .85 | 1.1  | 3.3 |
| LCX    |     |     |     |     |      | 3.3 |
| LV     | .4  | .8  | 1.5 | 2.0 | 2.4  | 3.3 |
| LVC    | .4  | .8  | 1.5 | 2.0 | 2.4  | 3.3 |
| LVQ    |     |     |     |     |      | 3.3 |
| LVT    | .4  | .8  | 1.5 | 2.0 | 2.4  | 3.3 |
| LVX    |     |     |     |     |      | 3.3 |
| SSTL   | 1.1 | 1.3 | 1.5 | 1.7 | 1.9  | 3.3 |
| VCX    |     |     |     |     |      | 3.3 |
| VHC    |     |     |     |     |      | 3.3 |
|        |     |     |     |     |      |     |
|        |     |     |     |     |      |     |

| <b>Family</b> | <b>Vol</b> | <b>Vil</b> | <b>Vt</b> | <b>Vih</b> | <b>Voh</b> | <b>Vcc</b> |
|---------------|------------|------------|-----------|------------|------------|------------|
| ALB           |            |            |           |            |            |            |
| ALVC          | .2         | .7         | 1.2       | 1.7        | 2.3        | 2.5        |
| ALVT          | .2         | .7         | 1.2       | 1.7        | 2.3        | 2.5        |
| F             |            |            |           |            |            |            |
| FAST          |            |            |           |            |            |            |
| HC            |            |            |           |            |            |            |
| LCX           |            |            |           |            |            |            |
| LVC           | .2         | .7         | 1.2       | 1.7        | 2.3        | 2.5        |
| VCX           |            |            |           |            |            | 2.5        |
|               |            |            |           |            |            |            |
|               |            |            |           |            |            |            |
| BTL           |            |            |           |            |            |            |
| ECL           |            |            |           |            |            |            |
| GTL<br>/GTL+  |            |            |           |            |            |            |
| LVDS          |            |            |           |            |            |            |

## Capabilities

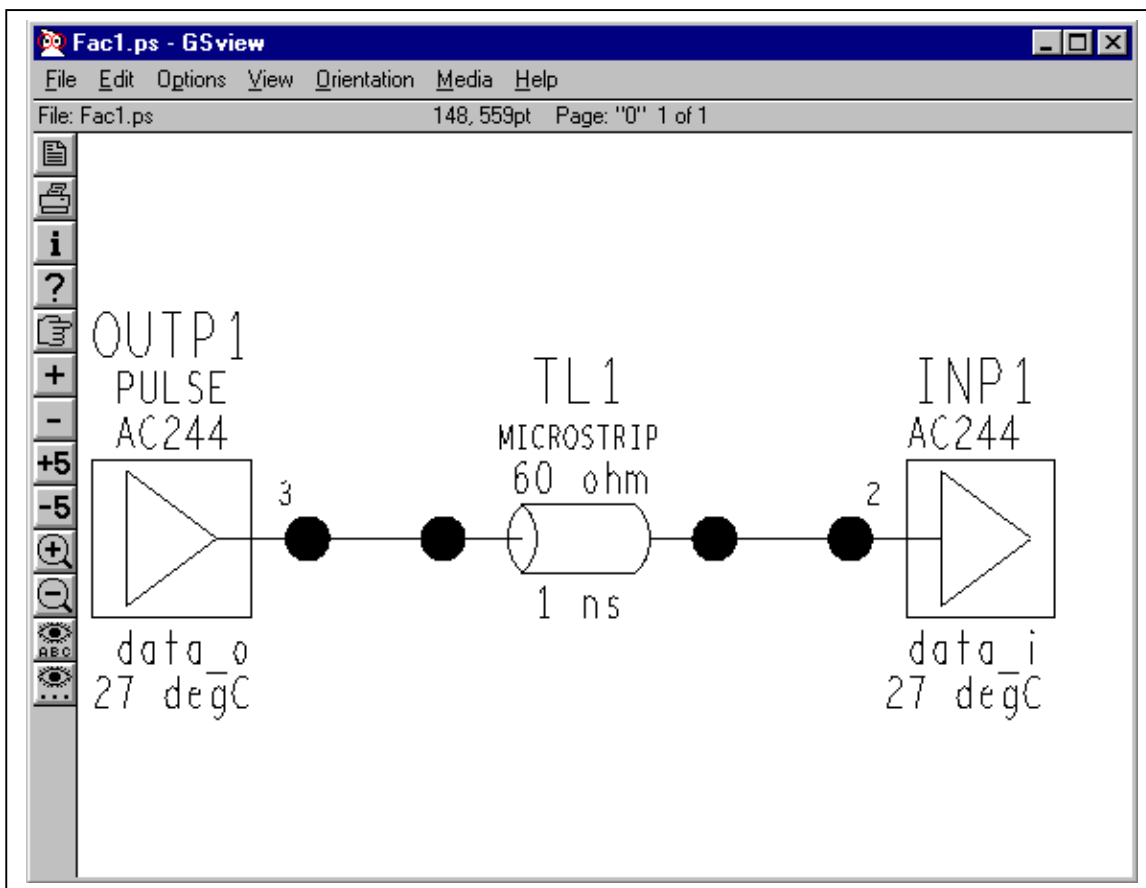
| Family   | Drive<br>$I_{ol}/I_{oh}$<br>mA | $t_{PD}$<br>nS | $t_r$<br>nS | $t_f$<br>nS | Supply<br>Current<br>$I_{cc}$ |
|----------|--------------------------------|----------------|-------------|-------------|-------------------------------|
| ABT      | 64/-32                         | 3.6            | 1.6         | 1.4         | 30 mA                         |
| AC       | 24/-24                         | 7.5            | 1.7         | 1.5         | 80 uA                         |
| ACQ      | 24/-24                         | 6.5            | 2.4         | 2.4         | 80 uA                         |
| ACT      | 24/-24                         | 10             | 1.7         | 1.5         | 80 uA                         |
| ACTQ     | 24/-24                         | 7              | 2.5         | 2.4         | 80 uA                         |
| AHC      | 8/-8 4/-4                      | 8.5/13.5       |             |             |                               |
| ALS      | 24/-15                         | 10             | 2.3         | 2.3         | 27 mA                         |
|          |                                |                |             |             |                               |
| ALVC     | 24/-24                         | 3              |             |             |                               |
| ALVT     | 64/-32                         |                |             |             |                               |
| AS       | 64/-15                         | 6.2            | 2.1         | 1.5         | 90 mA                         |
| FAST     | 64/-15                         | 6.5            | 2.3         | 2.3         | 90 mA                         |
| GTL/GTLP | 34/OD                          | 8.2-7.9        | 2.6         | 2.6         | 1.04 uA                       |
| HC       | 6/-6                           | 25             | 3.6         | 4.1         | 80 uA                         |
| HCT      | 6/-6                           | 25             | 4.6         | 3.9         | 80 uA                         |
| LCX      | 24/-24                         | 4.5            | 2.9         | 2.4         | 20 uA                         |
| LS       | 24/-15                         | 18             |             |             | 54 mA                         |
|          |                                |                |             |             |                               |
| LVC      | 24/-24                         | 6.5            |             |             |                               |
| LVQ      | 12/-12                         | 9.5            | 3.5         | 3.2         | 40 uA                         |
| LVT      | 64/-32                         | 4.1            | 2.4         | 2.2         | 9.5 mA                        |
| LVX      | 4/-4                           | 12             | 4.8         | 3.7         | 40 uA                         |
| S        | 64/-15                         | 9              |             |             | 120 mA                        |
| SSTL     | 20/-20                         |                |             |             |                               |
| TTL      | 40/.25                         | 30             |             |             | 41 mA                         |
|          |                                |                |             |             |                               |
| VCX      | 24/-24                         | 2.5/3.2        | 2.4 / 3.1   | 2.1/2.5     | 20 uA                         |
| VHC      | 8/-8                           | 8.5            | 4.1         | 3.2         | 40 uA                         |
| VHCT     | 8/-8                           | 9.5            |             |             | 40 uA                         |
|          |                                |                |             |             |                               |

## Test Circuit Examples

General Simulation Settings:

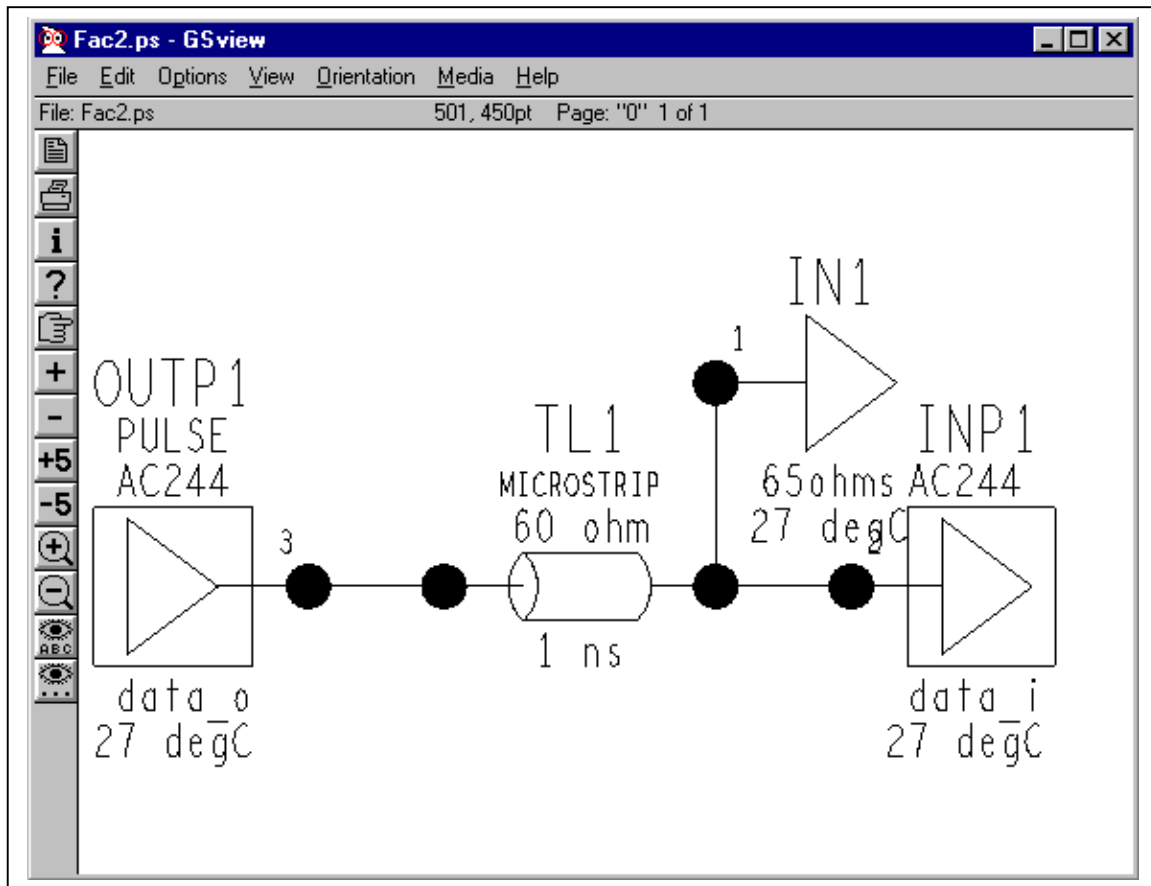
Most reflection simulations were done at 50 MHz and 1 cycle with the Typical IBIS model selected. The transmission line was set at  $Z_0 = 60$  ohms and 1 nS delay.

Unterminated





Terminated

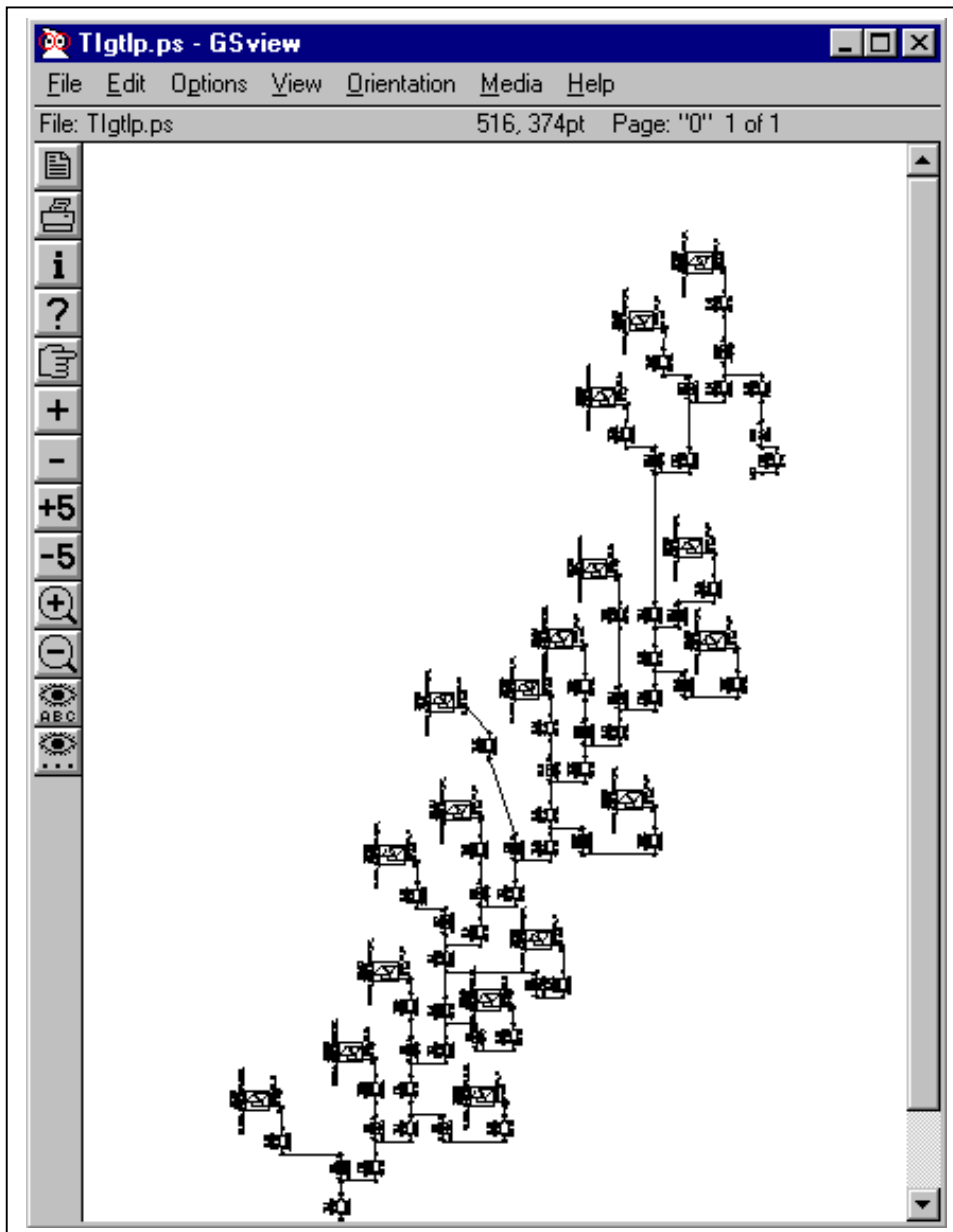


For terminations a V-I curve with  $R_{in} = R_L = 65 \text{ ohms}$  was used. This provides a small, non-zero reflection at the receiver:

$$\rho = \frac{R_L - Z_0}{R_L + Z_0}$$

So, depending on input capacitance of the receiver and the frequency content of the driver, reflection coefficient ("matched") will be around 0.04.

## 18 Board Backplane



Pitch = 957 mils, Stubs = 1500 mils,  $f = 8.162$  MHz, Driver = slot 9, Pullups = 30 Ohms,  
 $Z_o = 63$  ohms,  $V_{pullup} = 1.5$  Volts

## Logic Family Results

### 5 Volt Logic

CMOS: , [CDS Default](#), AC, ACQ ACT, ACTQ, AHC, AHCT, HC, HCT, VHC, VHCT

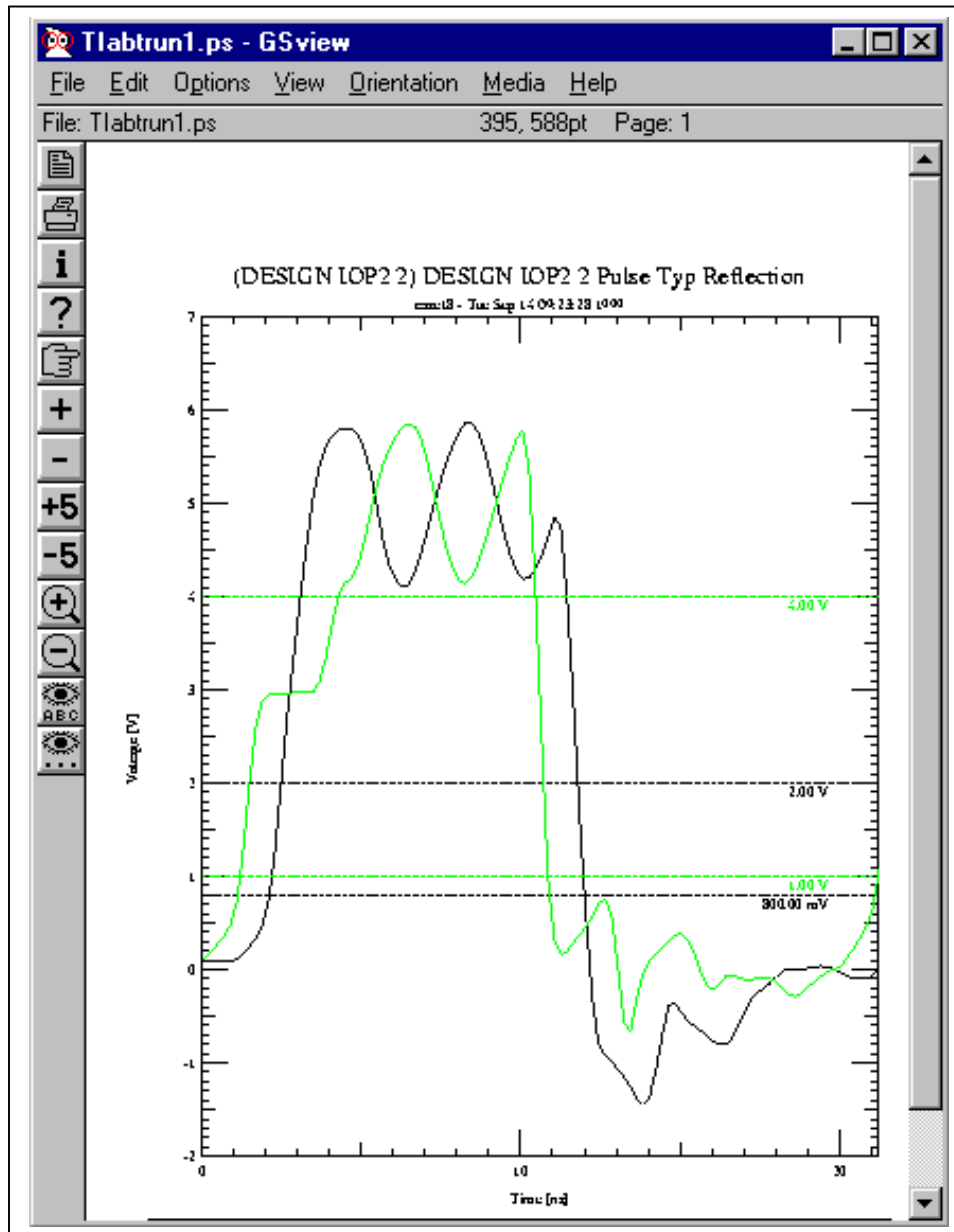
BiCMOS: ABT, ABTE

TTL (BP): ALS, AS, F, LS, S, TTL

## ABT: Advanced BiCMOS Technology

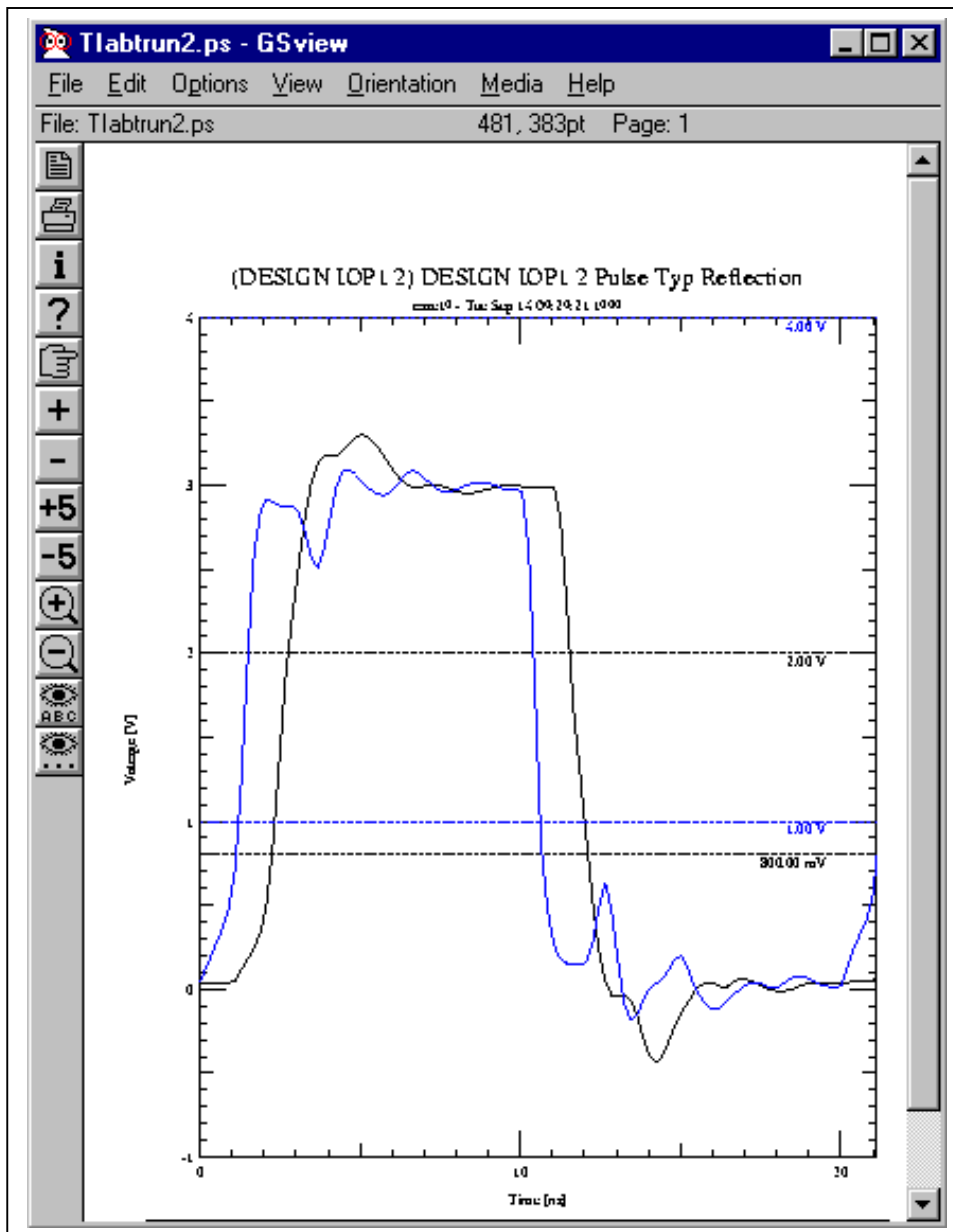
TI 0.8- $\mu$

Un-Terminated



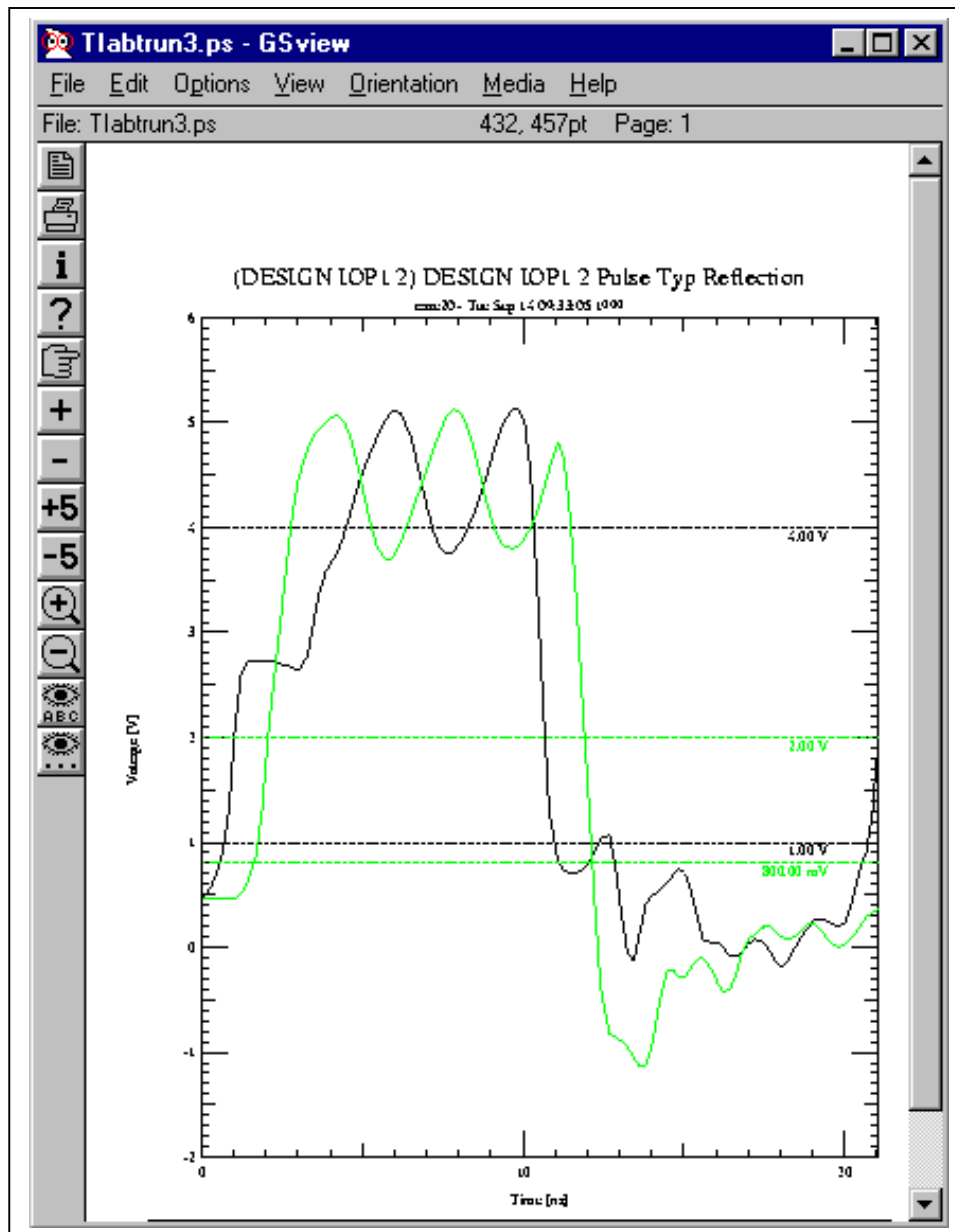
TI ABT: Driver = ABT16245a\_IO, Receiver = ABT16245a\_IO  
Run1

Terminated



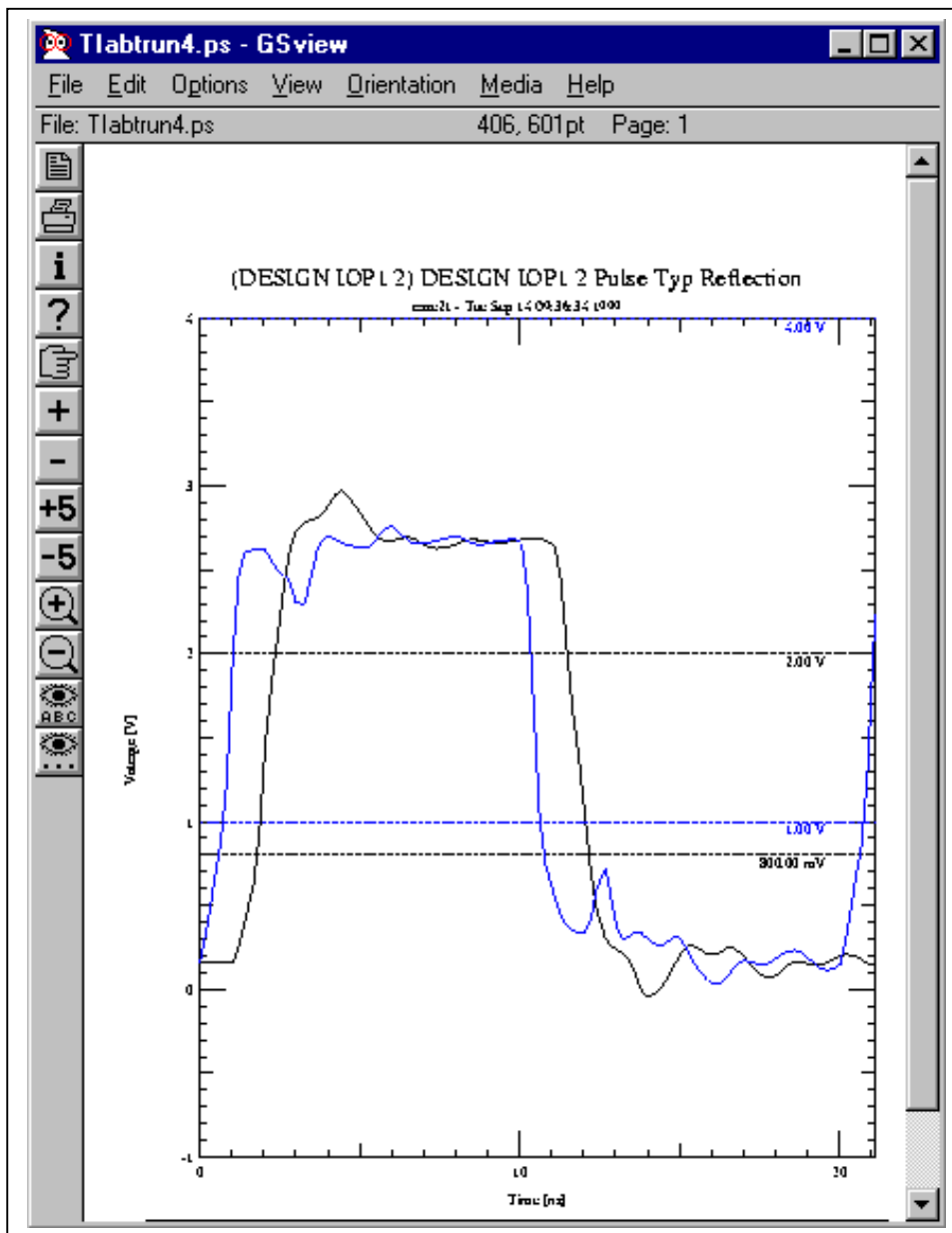
TI ABT: Driver = ABT16245a\_IO, Receiver = ABT16245a\_IO  
Run2

Un-Terminated



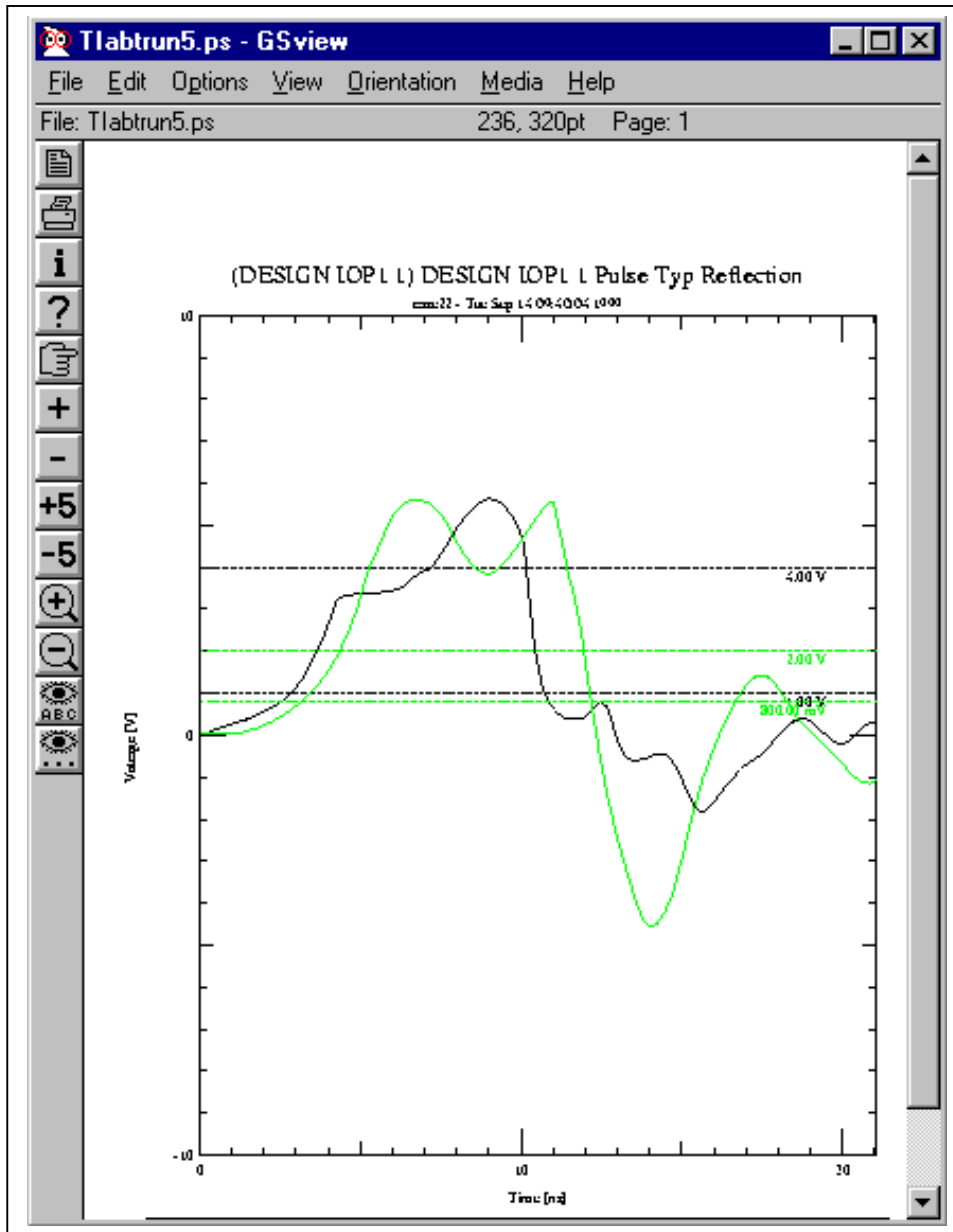
TI ABT: Driver = ABT245a\_IO, Receiver = ABT245a\_IO  
Run3

Terminated



TI ABT: Driver = ABT245a\_IO, Receiver = ABT245a\_IO  
Run4

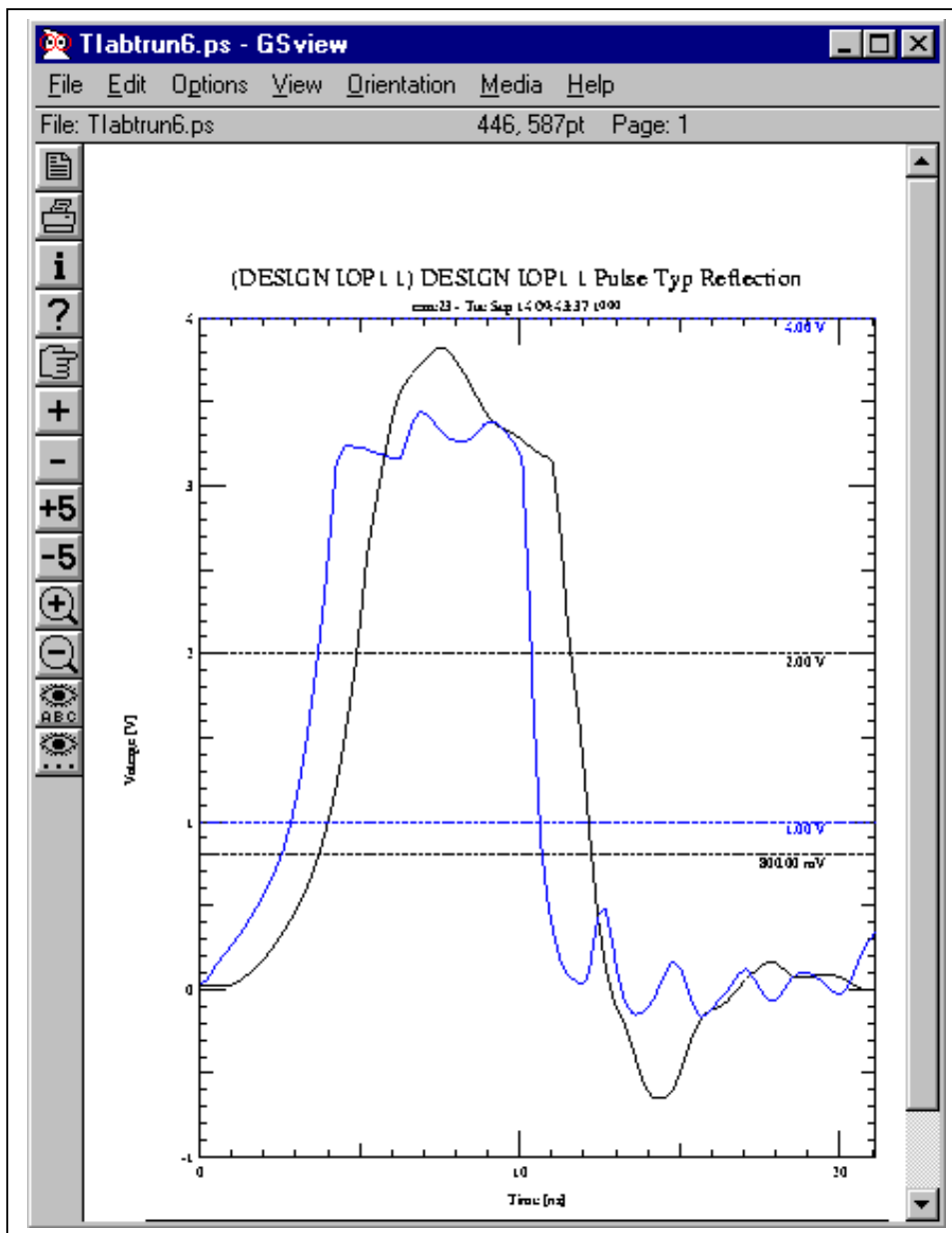
Un-Terminated



TI ABT: Driver = ABT25245\_A\_port (IO), Receiver = ABT25245\_A\_port (IO)  
Run5

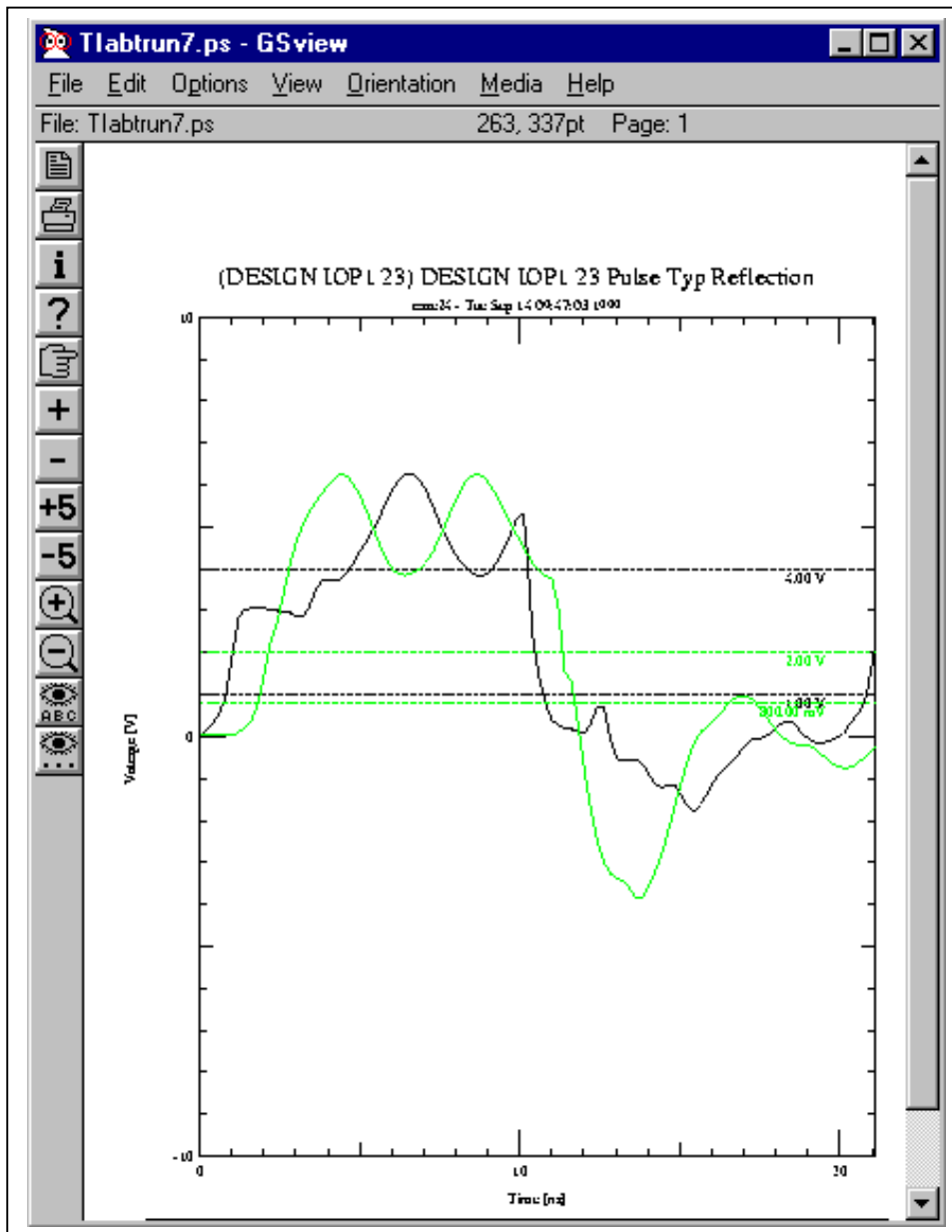


Terminated



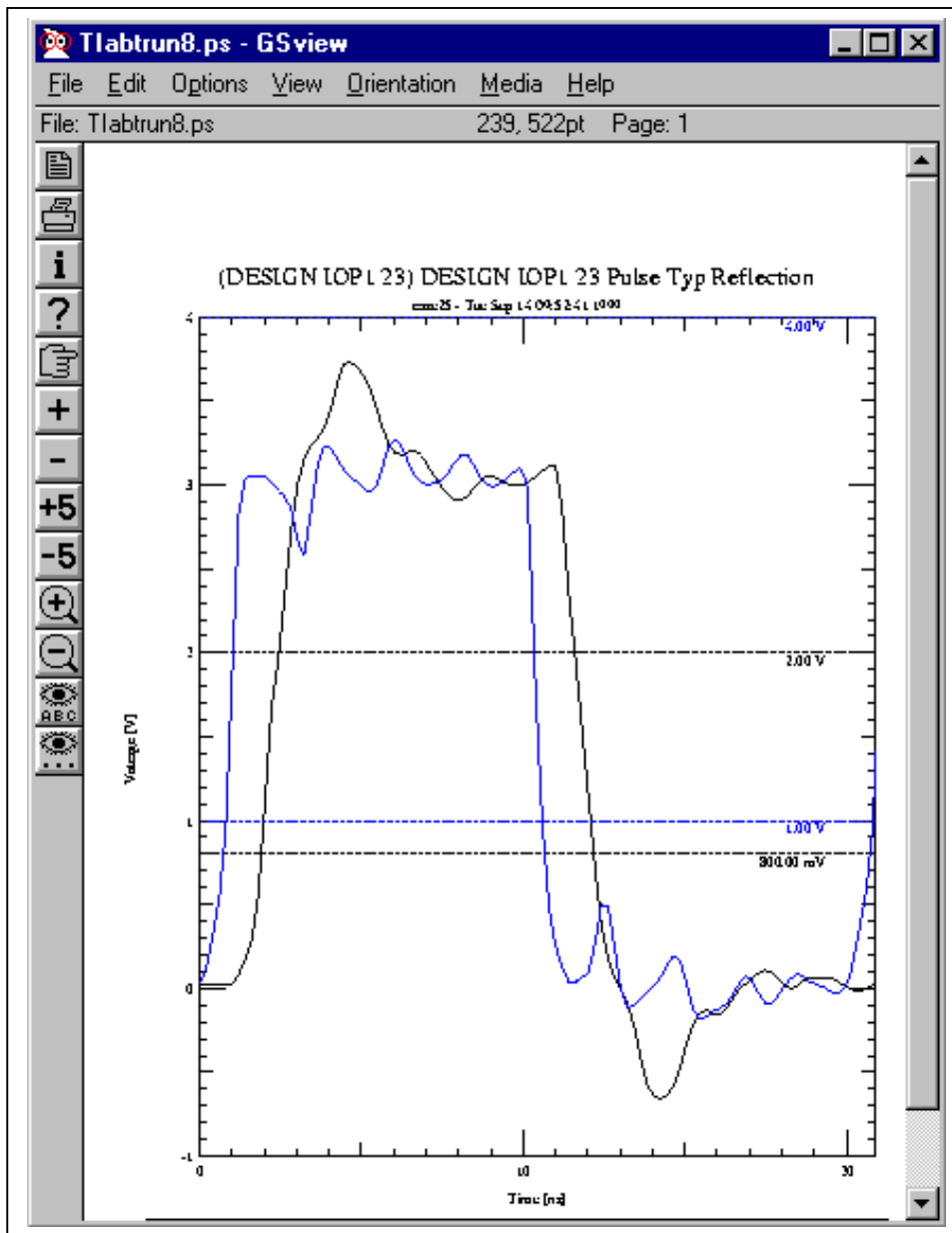
TI ABT: Driver = ABT25245\_A\_port (IO), Receiver = ABT25245\_A\_port (IO)  
Run6

Un-Terminated



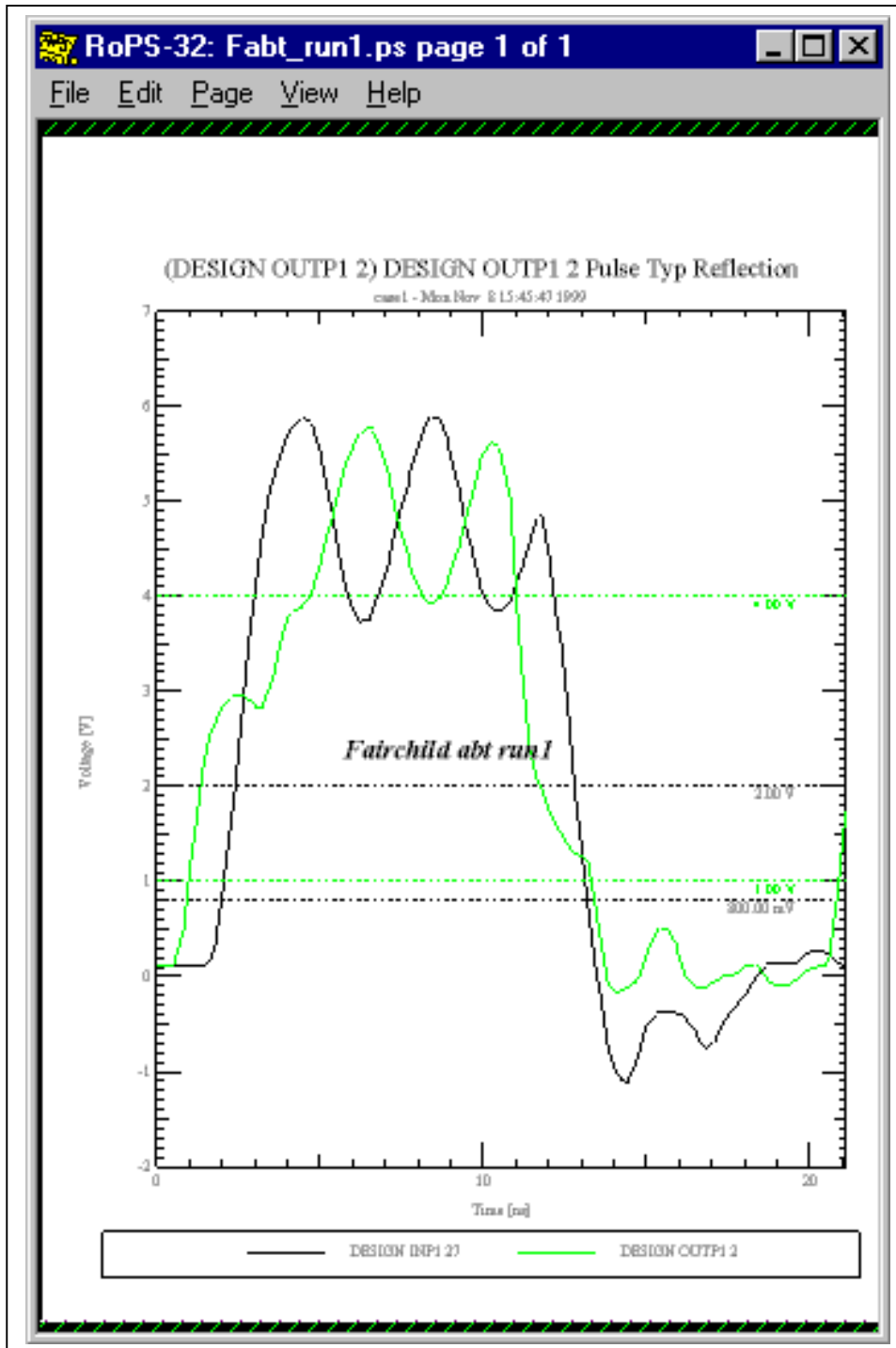
TI ABT: Driver = ABT25245\_B\_port (IO), Receiver = ABT25245\_B\_port (IO)  
Run7

Terminated



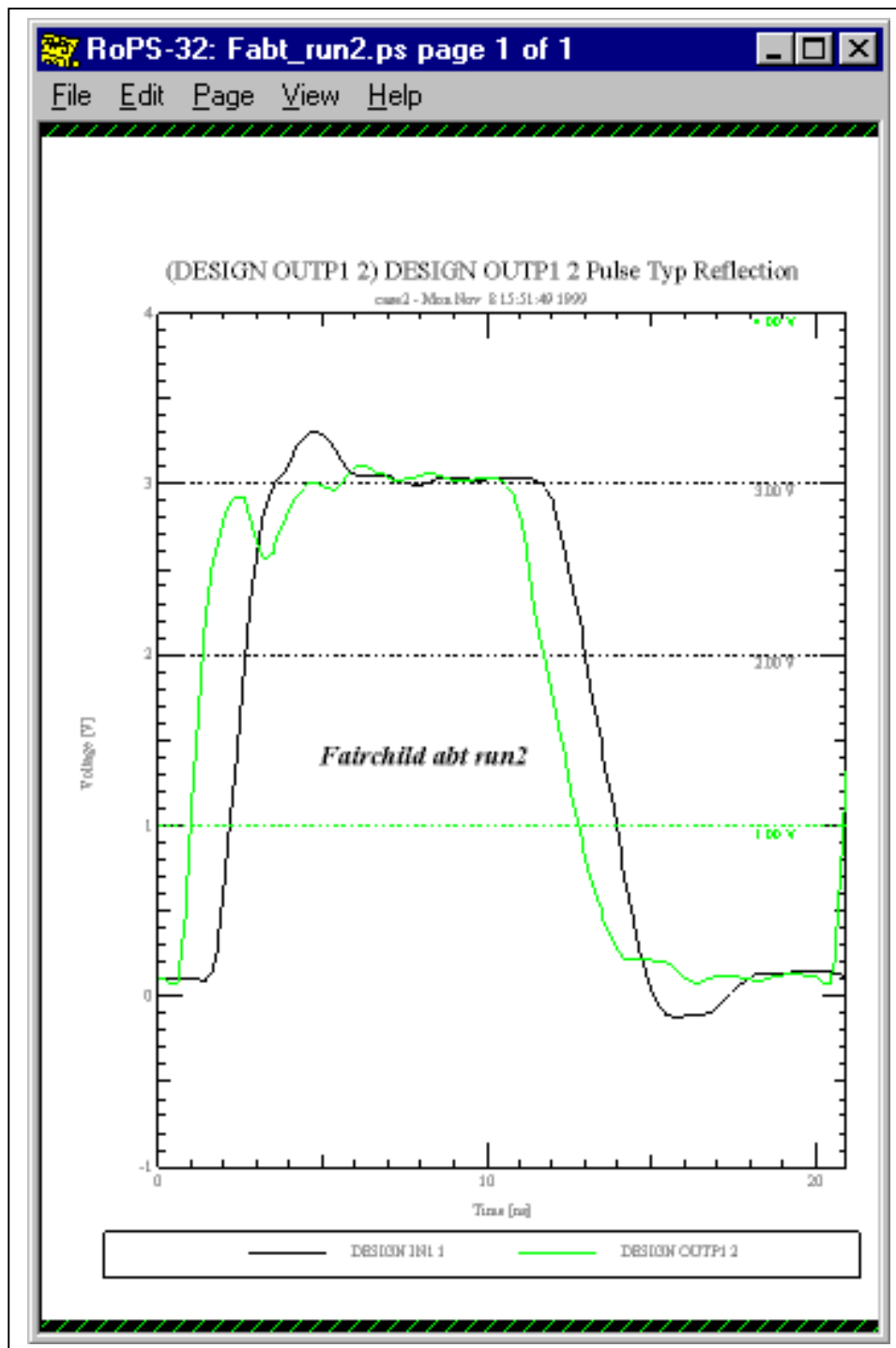
TI ABT: Driver = ABT25245\_B\_port (IO), Receiver = ABT25245\_B\_port (IO)  
Run8

Un-Terminated



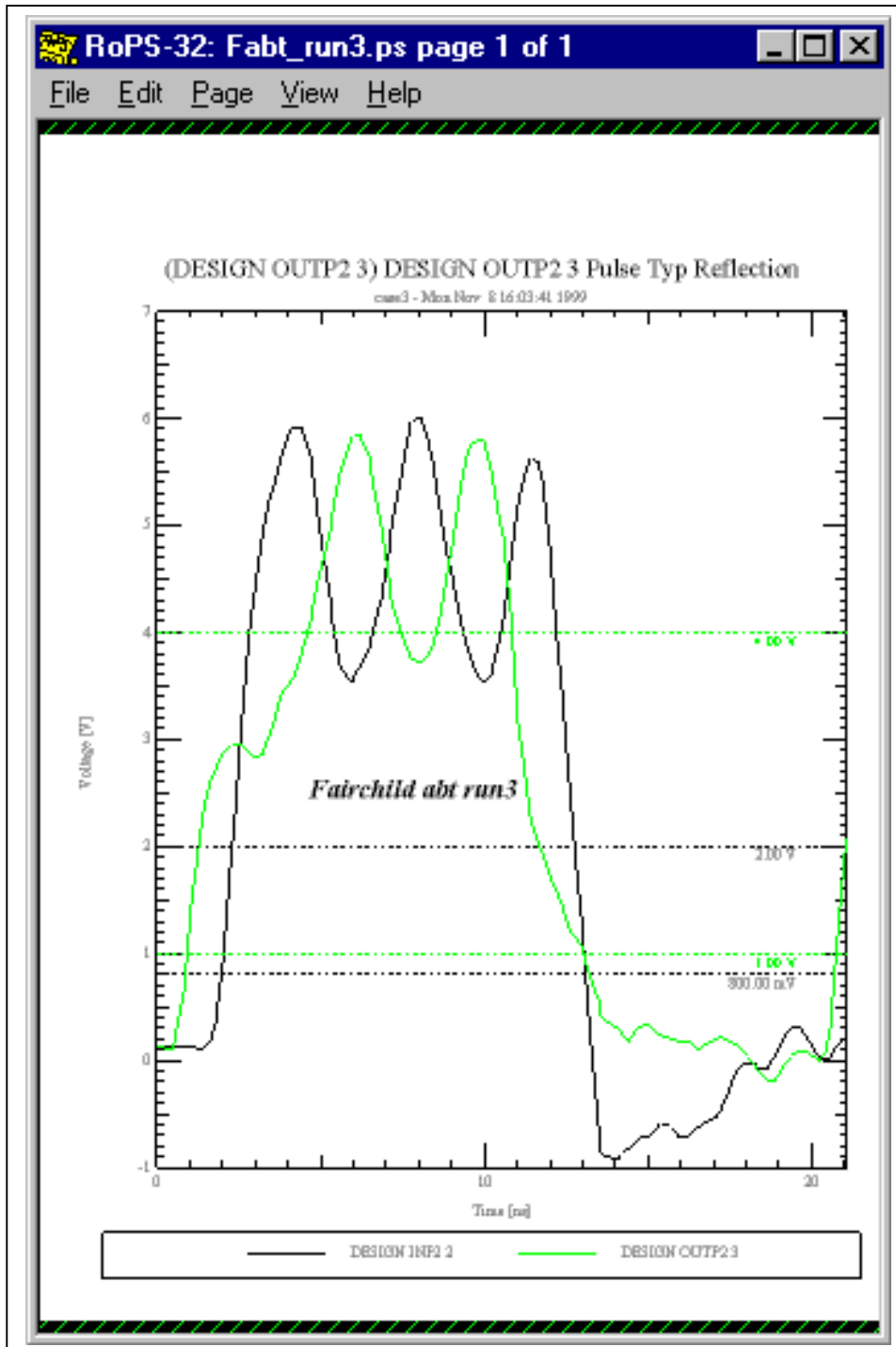
Fairchild ABT: Driver = ABT16244\_data\_o, Receiver = ABT16244\_data\_i  
Run1

Terminated



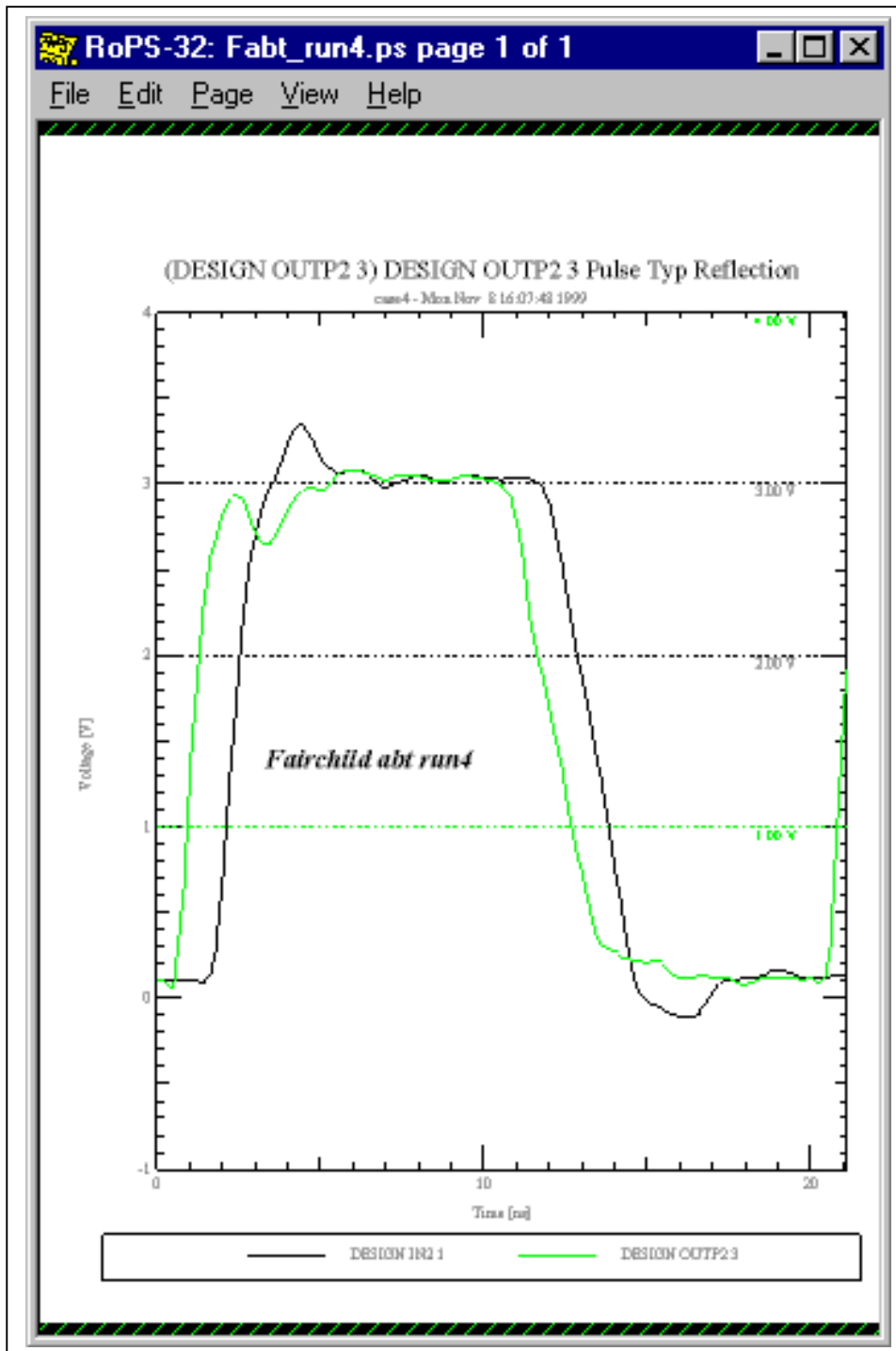
Fairchild ABT: Driver = ABT16244\_data\_o, Receiver = ABT16244\_data\_i  
Run2

Un-Terminated



Fairchild ABT: Driver = ABT244\_data\_o, Receiver = ABT244\_data\_i  
Run3

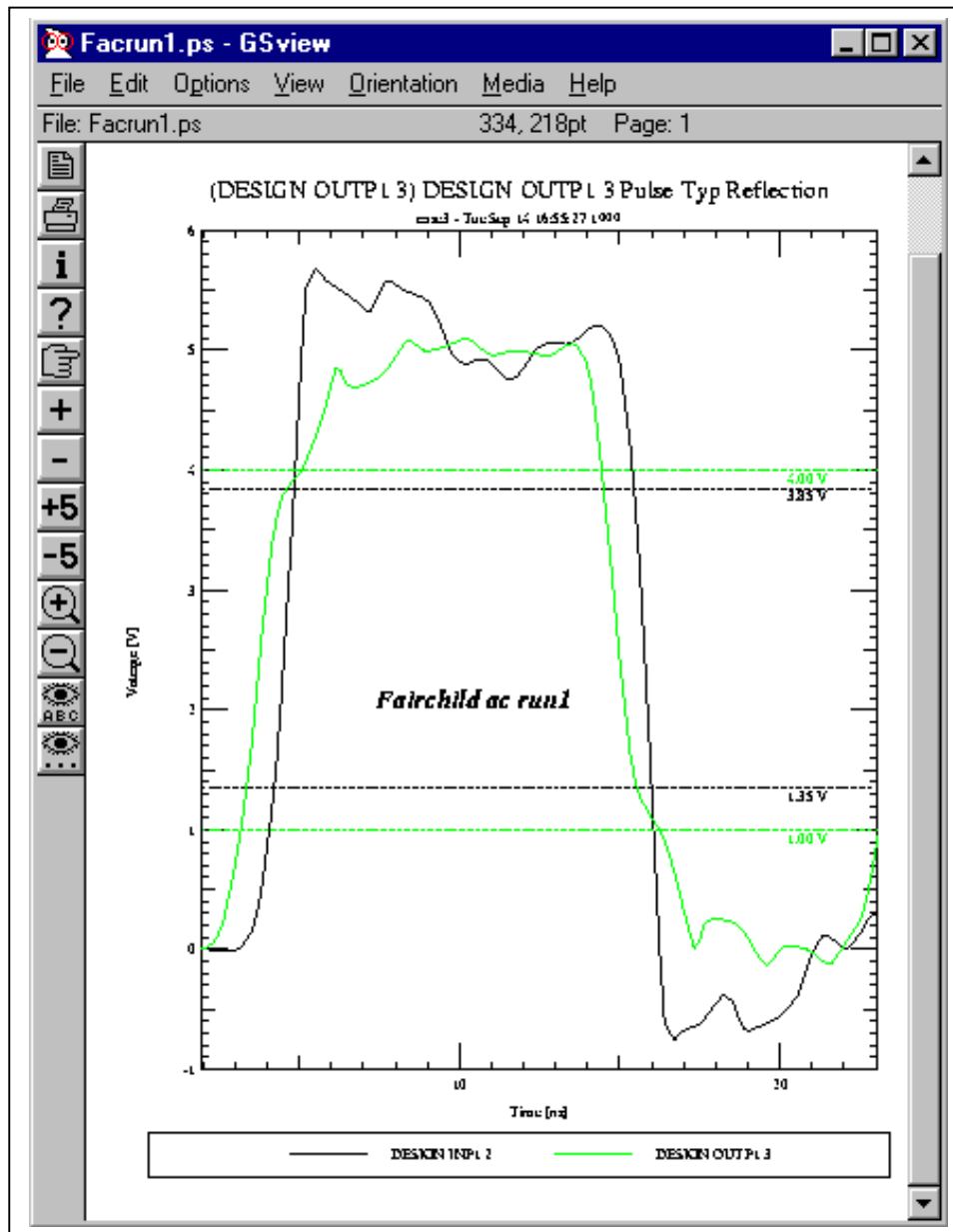
Terminated



Fairchild ABT: Driver = ABT244\_data\_o, Receiver = ABT244\_data\_i  
Run4

## AC: Advanced CMOS Logic TI, Fairchild

Un-Terminated

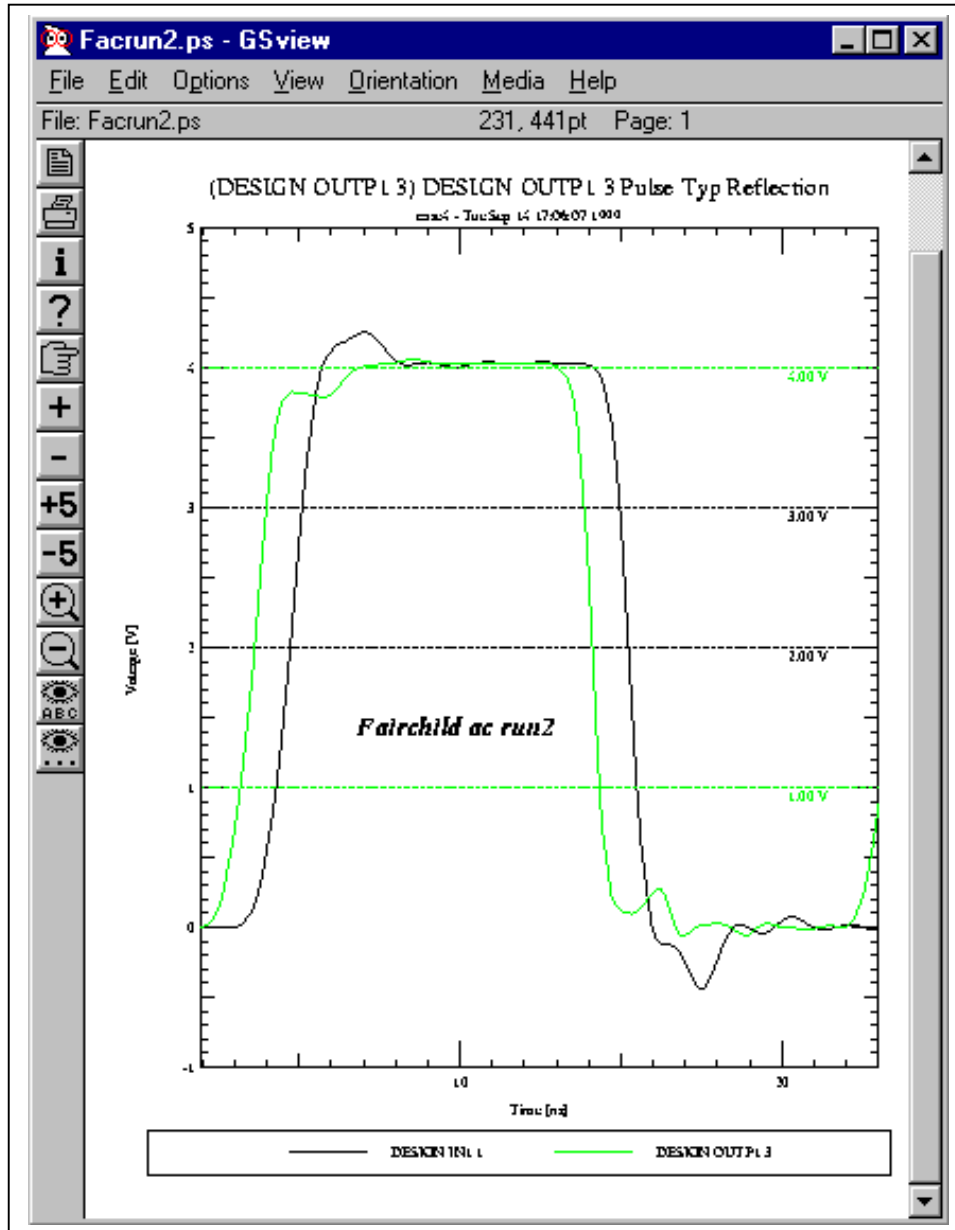


Fairchild AC: Driver = AC244 data\_o, Receiver = AC244 data\_i  
Run1

Terminated



Terminated

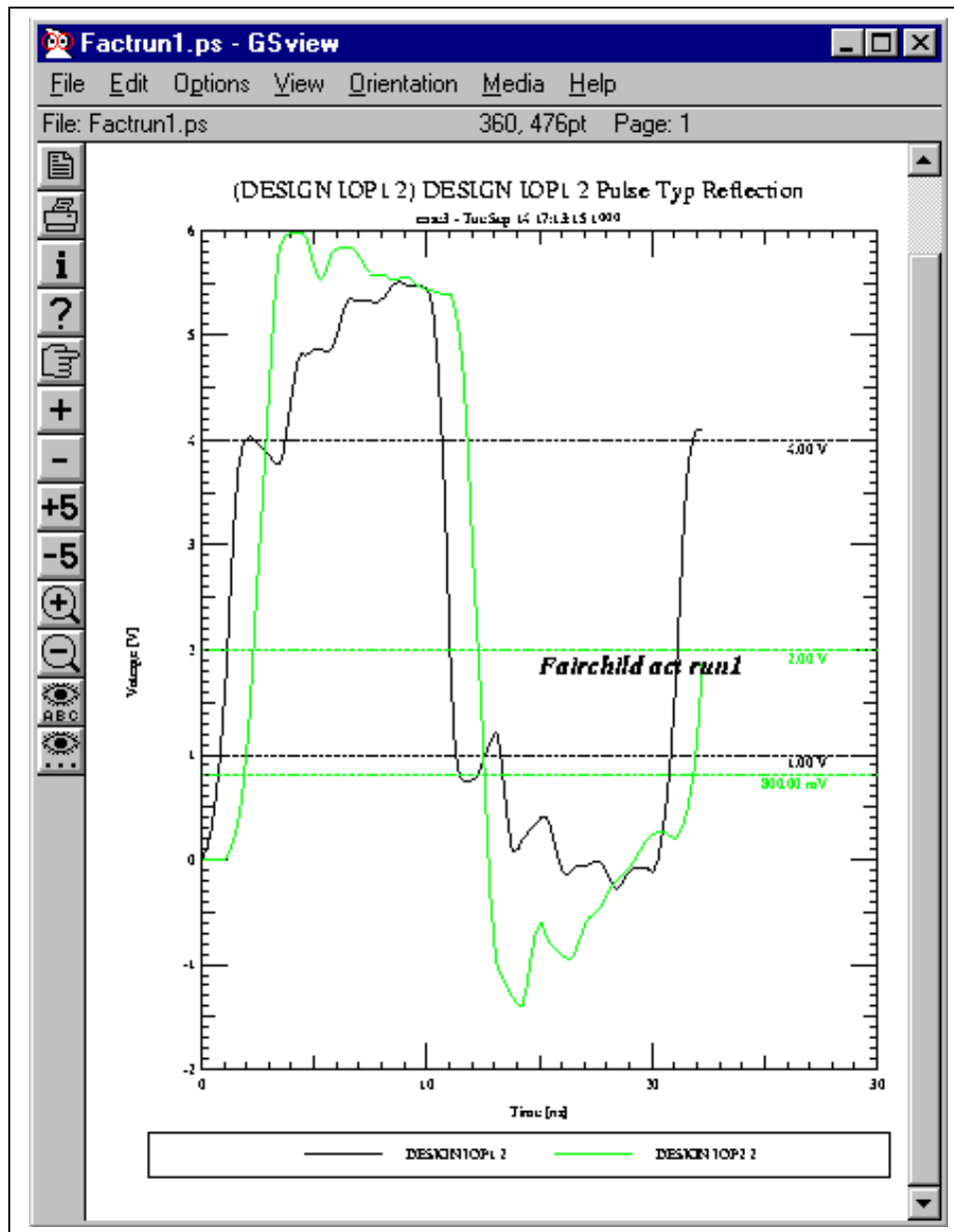


Fairchild AC: Driver = AC244 data\_o, Receiver = AC244 data\_i  
Run2

## ACT: Advanced CMOS Logic

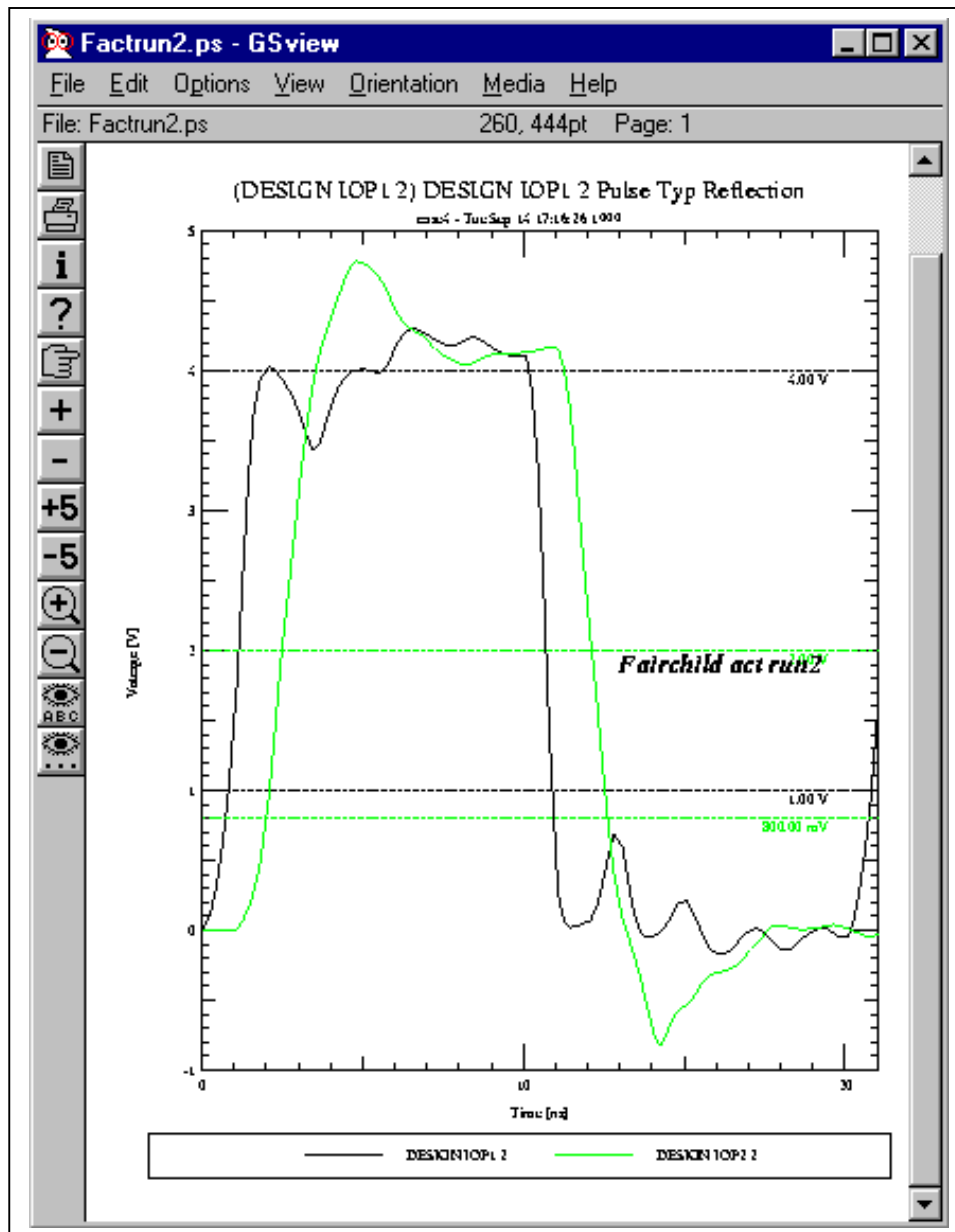
Fairchild

Un-Terminated



Fairchild ACTQ: Driver = 74ACT245SC data\_io, Receiver = 74ACT245SC data\_io  
Run1

Terminated

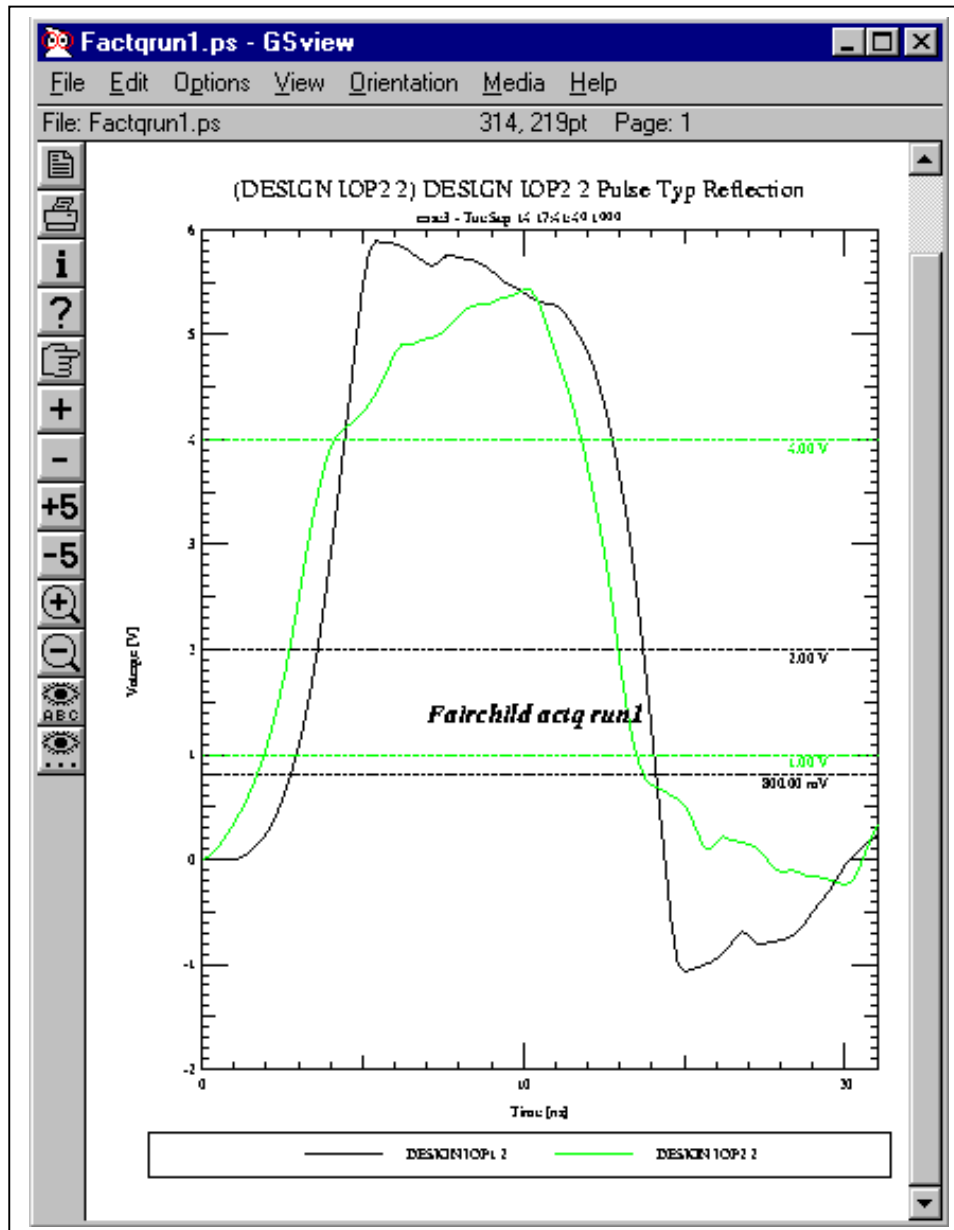


Fairchild ACT: Driver = 74ACTQ245SC data\_io, Receiver = 74ACT245SC data\_io  
Run2

## ACTQ: Advanced CMOS Logic

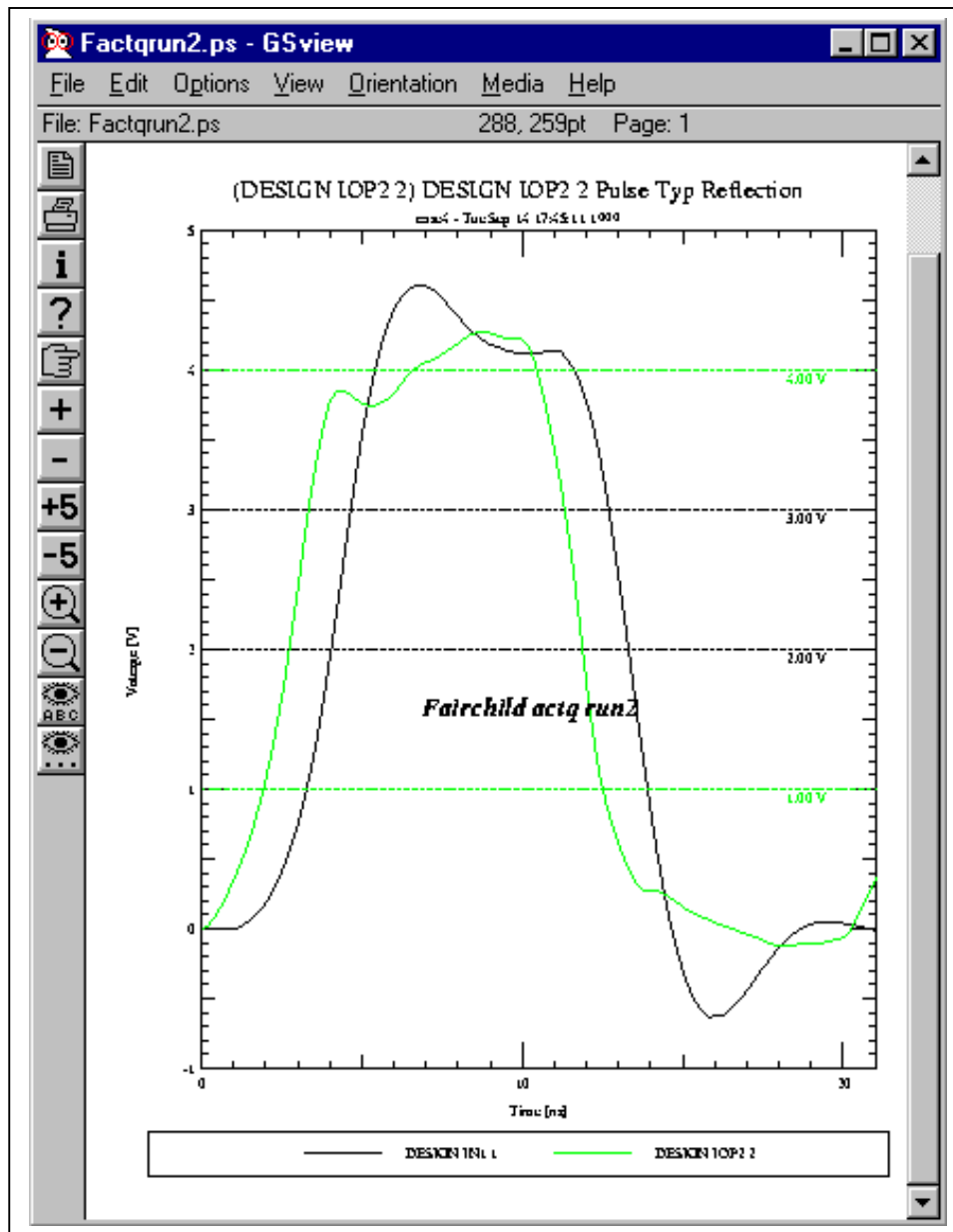
Fairchild

Un-Terminated



Fairchild ACTQ: Driver = 74ACTQ245SC data\_io, Receiver = 74ACTQ245SC data\_io  
Run1

Terminated

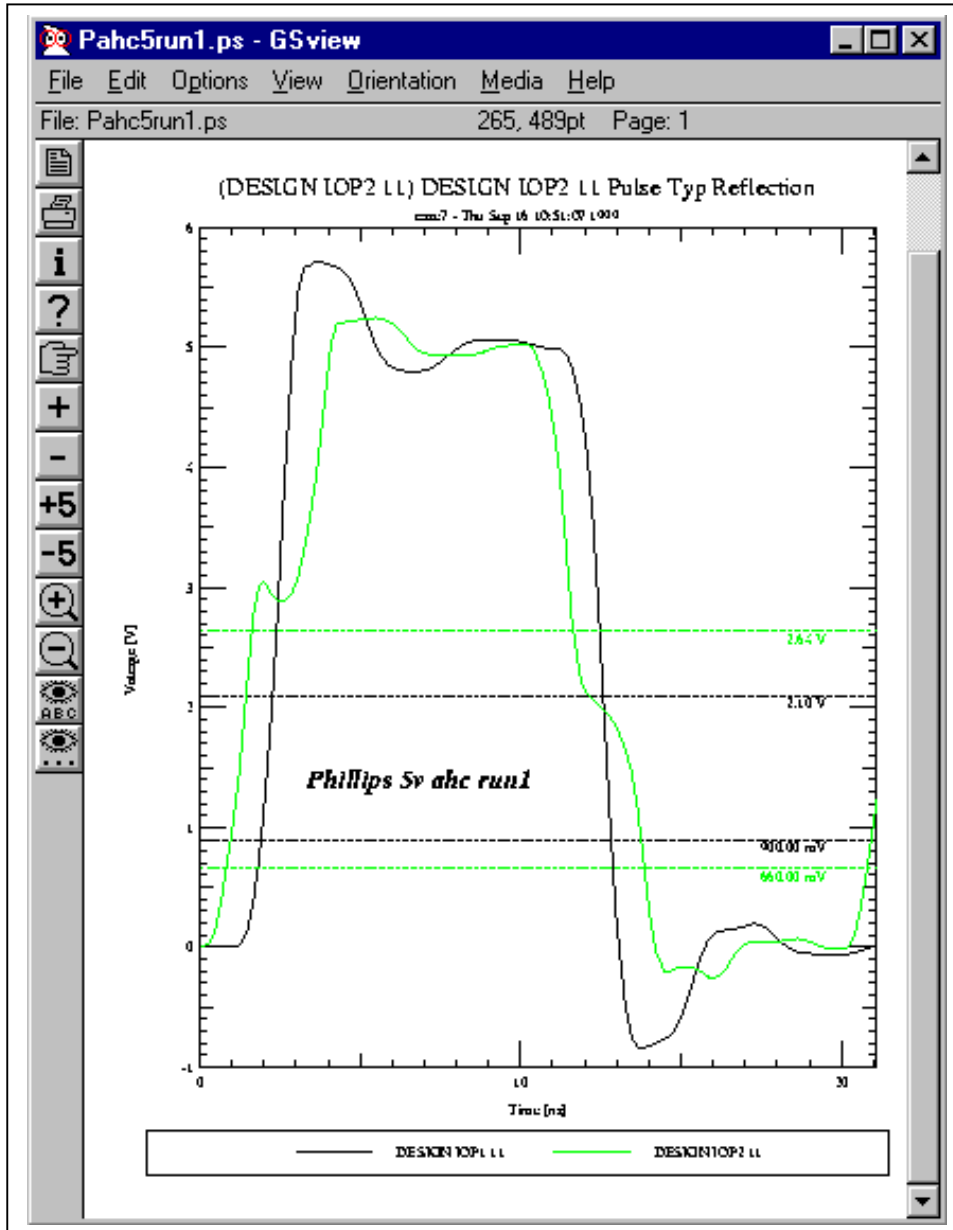


Fairchild ACTQ: Driver = 74ACTQ245SC data\_io, Receiver = 74ACTQ245SC data\_io  
Run2

## AHC: Advanced High Speed CMOS Logic

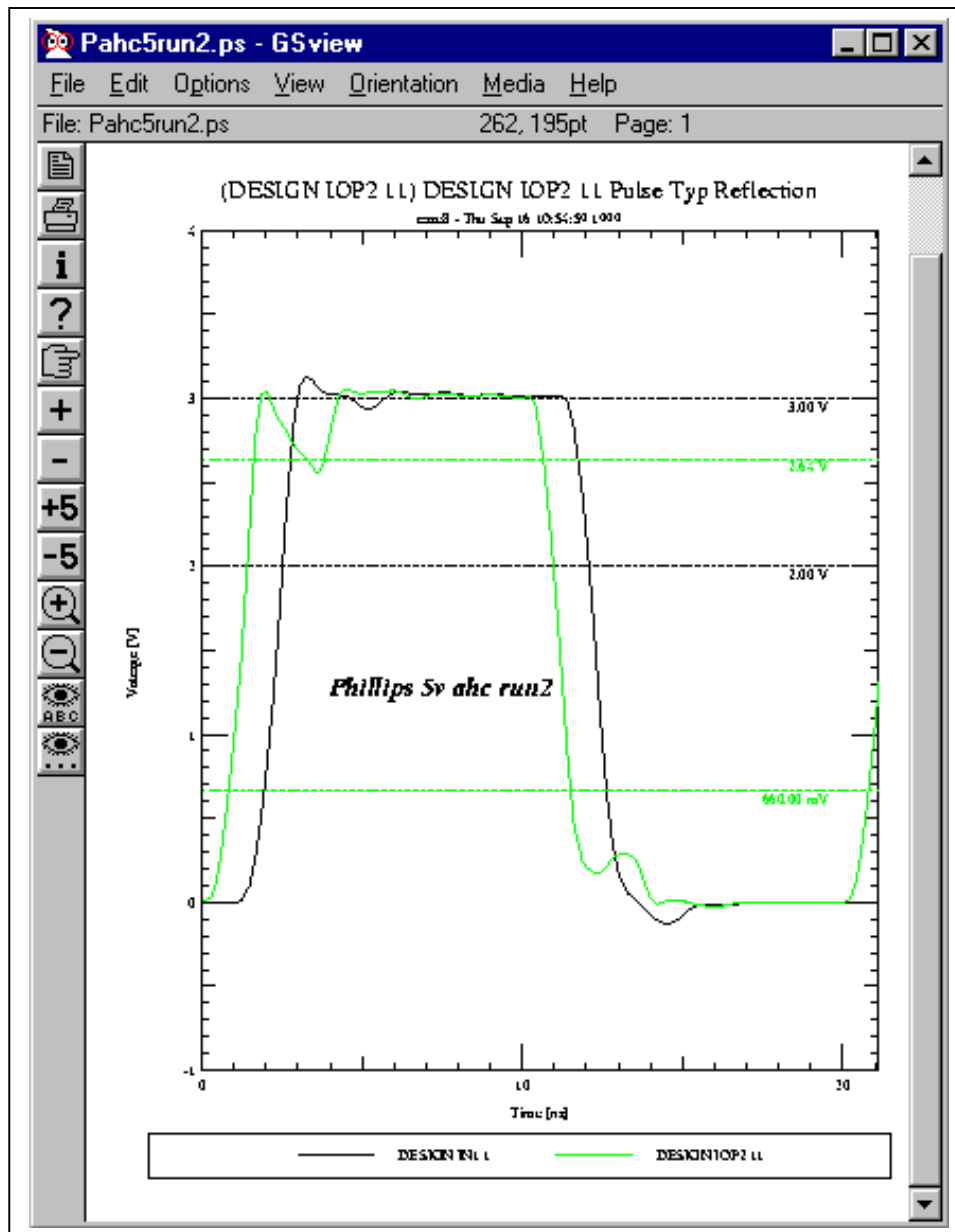
TI, Phillips

Un-Terminated



Phillips AHC: Driver = 74AHC245\_IO\_5V, Receiver = 74AHC245\_IO\_5V  
Run1

Terminated

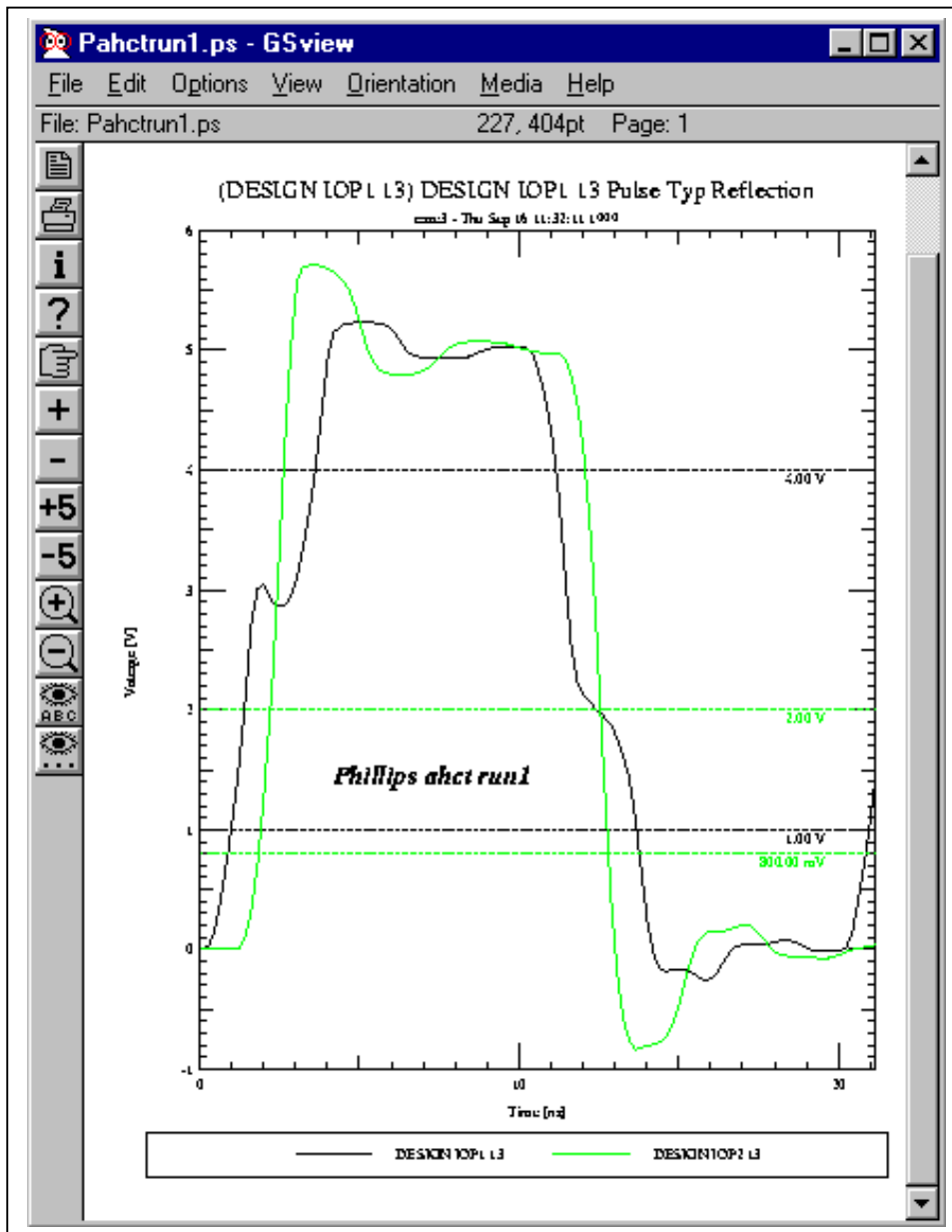


Phillips AHC: Driver = 74AHC245\_IO\_3V, Receiver = 74AHC245\_IO\_3V  
Run2

## AHCT: Advanced High Speed CMOS Logic

TI, Phillips

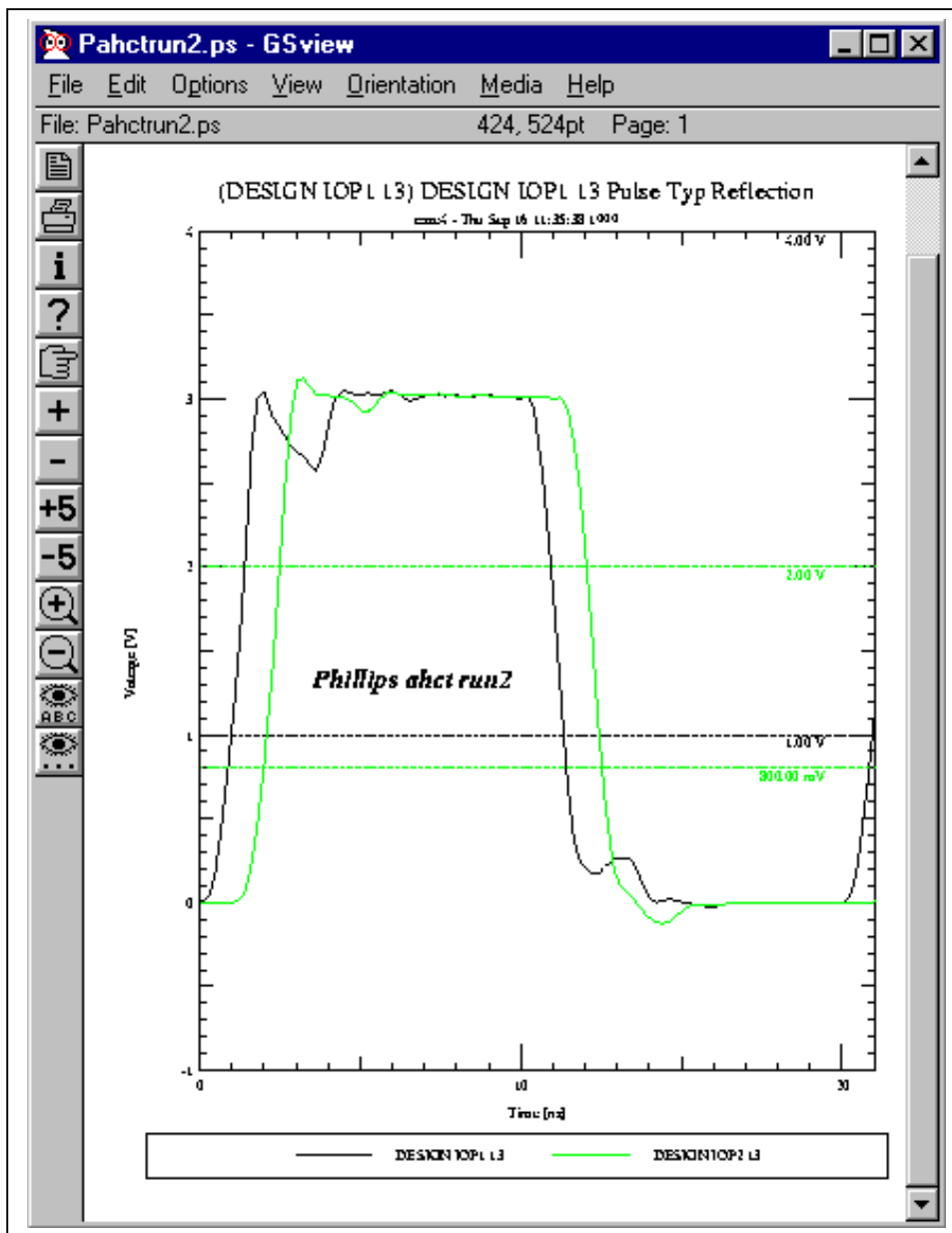
Un-Terminated



Phillips: Driver = 74AHCT245 IO\_TTL, Receiver = 74AHCT245 IO\_TTL  
Run1



Terminated



Phillips: Driver = 74AHCT245 IO\_TTL, Receiver = 74AHCT245 IO\_TTL  
Run1

**\*ALS**

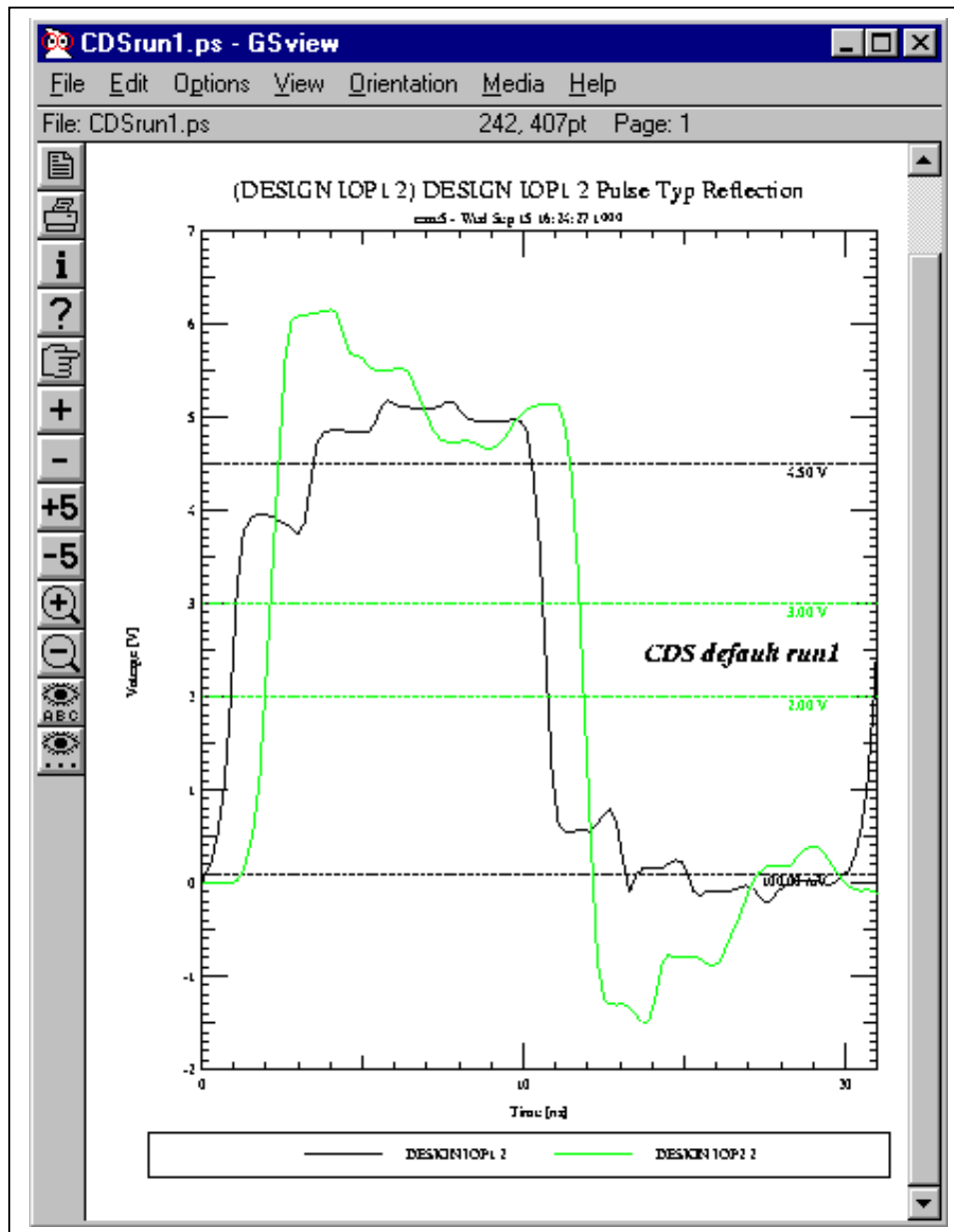
Advanced Low Power Schottky Logic  
TI

**\*AS**

Advanced Schottky Logic  
TI

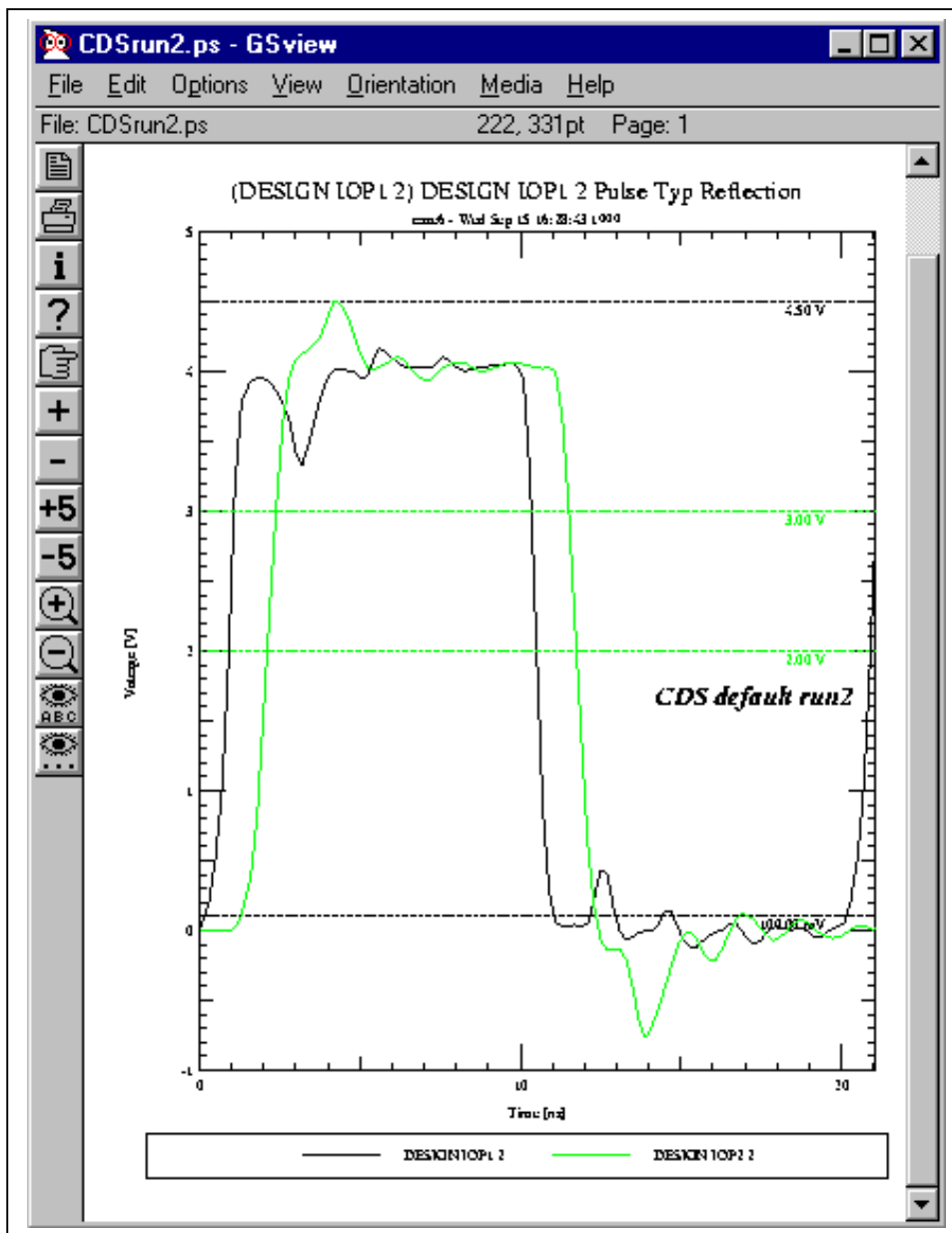
## CDS Default: Cadence Design Systems CMOS Default

Un-Terminated



CDS Default: Driver = CDSDefaultIO, Receiver = CDSDefaultIO  
Run1

Terminated

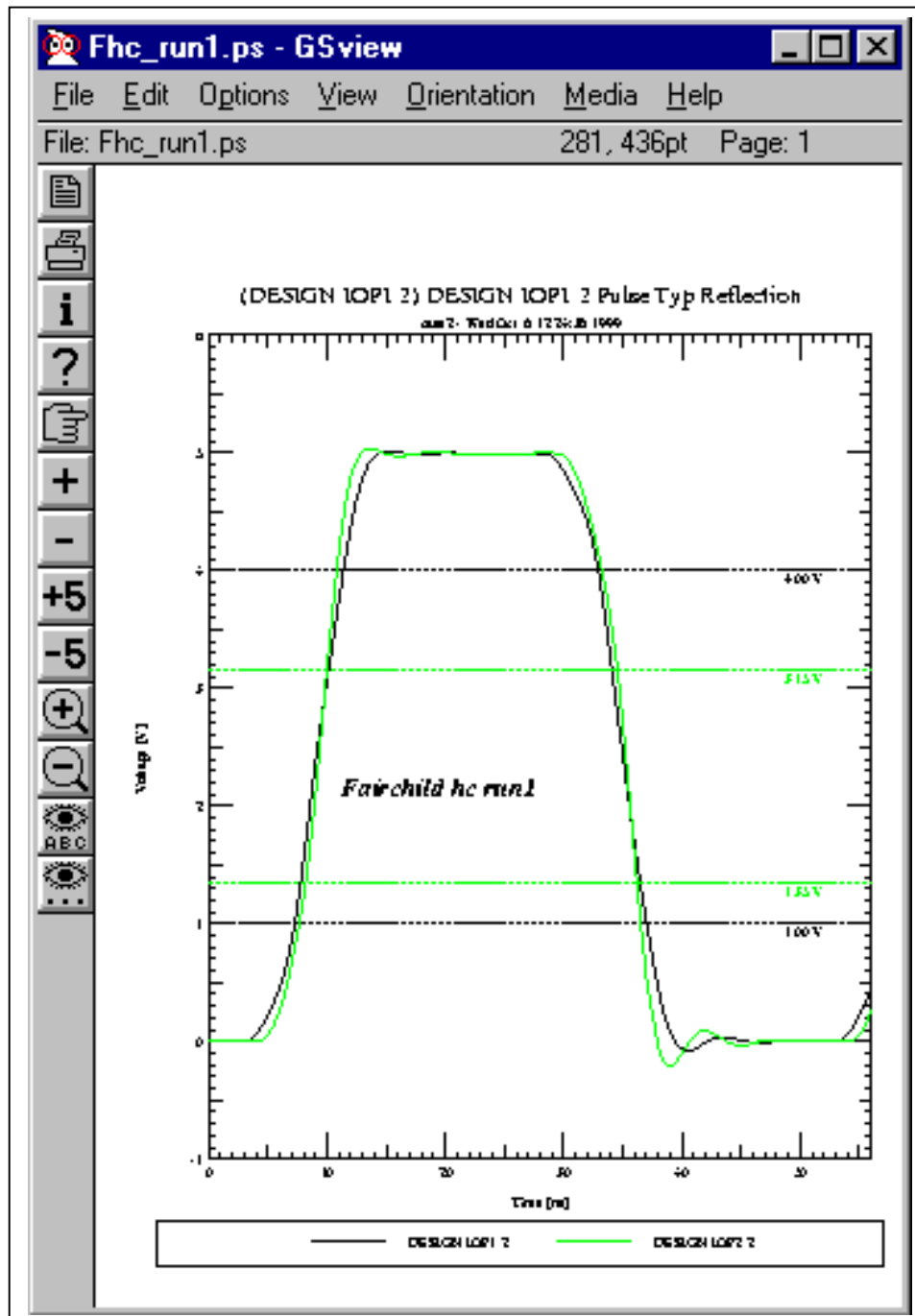


CDS Default: Driver = CDSDefaultIO, Receiver = CDSDefaultIO  
Run1

## HC: High Speed CMOS Logic

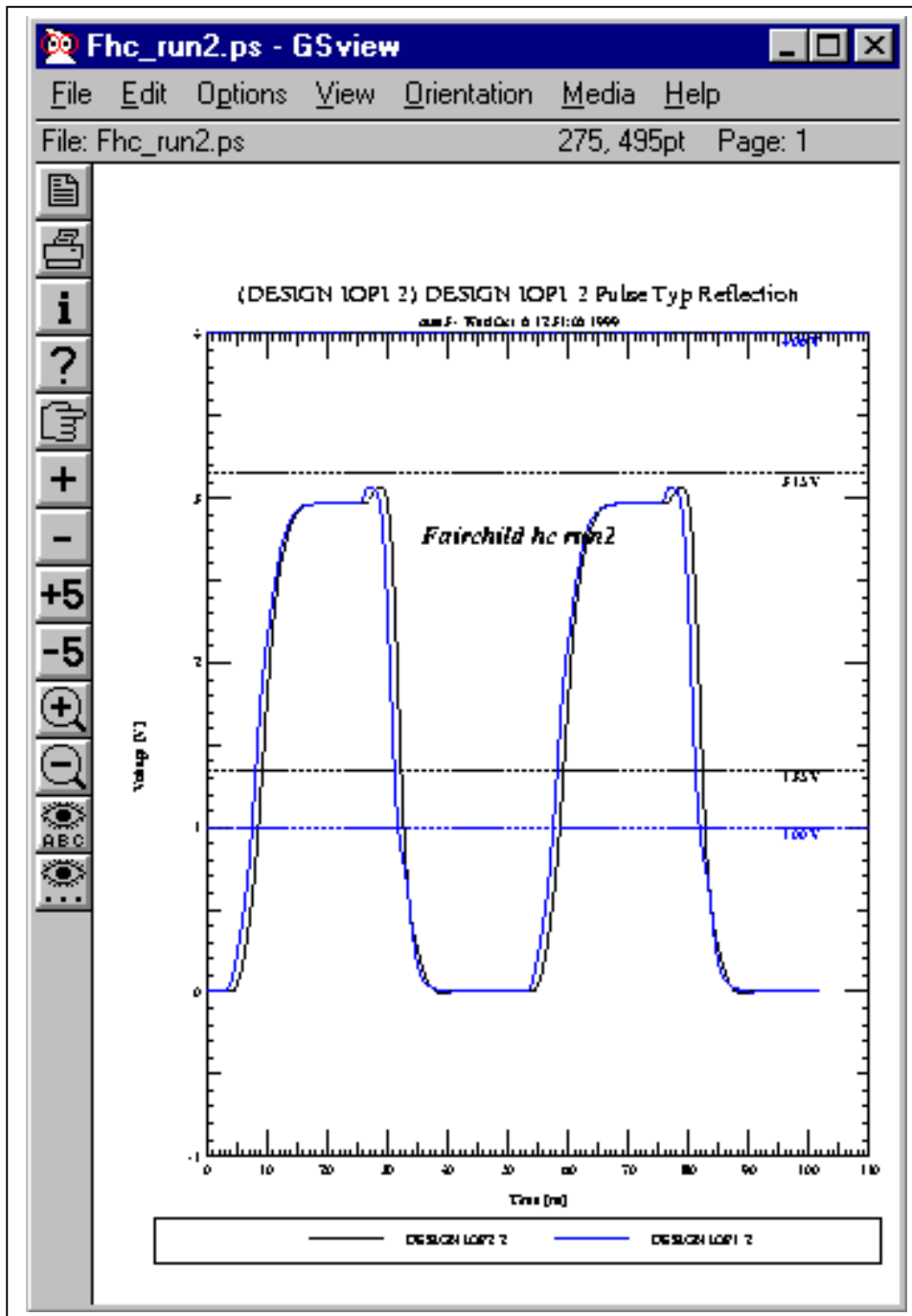
Fairchild

Un-Terminated



Fairchild HC: Driver = 74HC245SC data\_io, Receiver = 74HC245SC data\_io  
Run1

Terminated

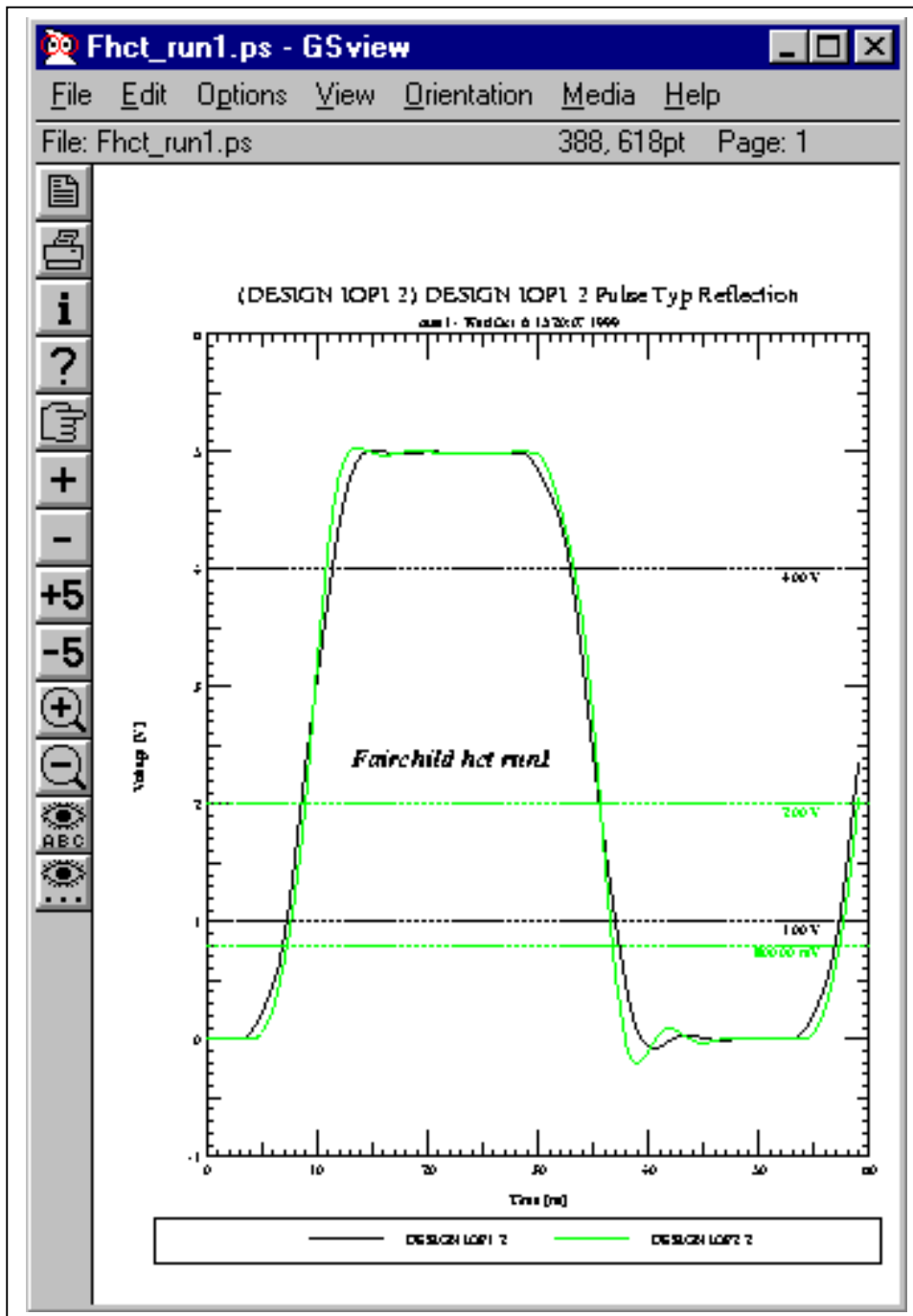


Fairchild HC: Driver = 74HC245SC data\_io, Receiver = 74HC245SC data\_io  
Run2

## HCT: High Speed CMOS Logic

Fairchild

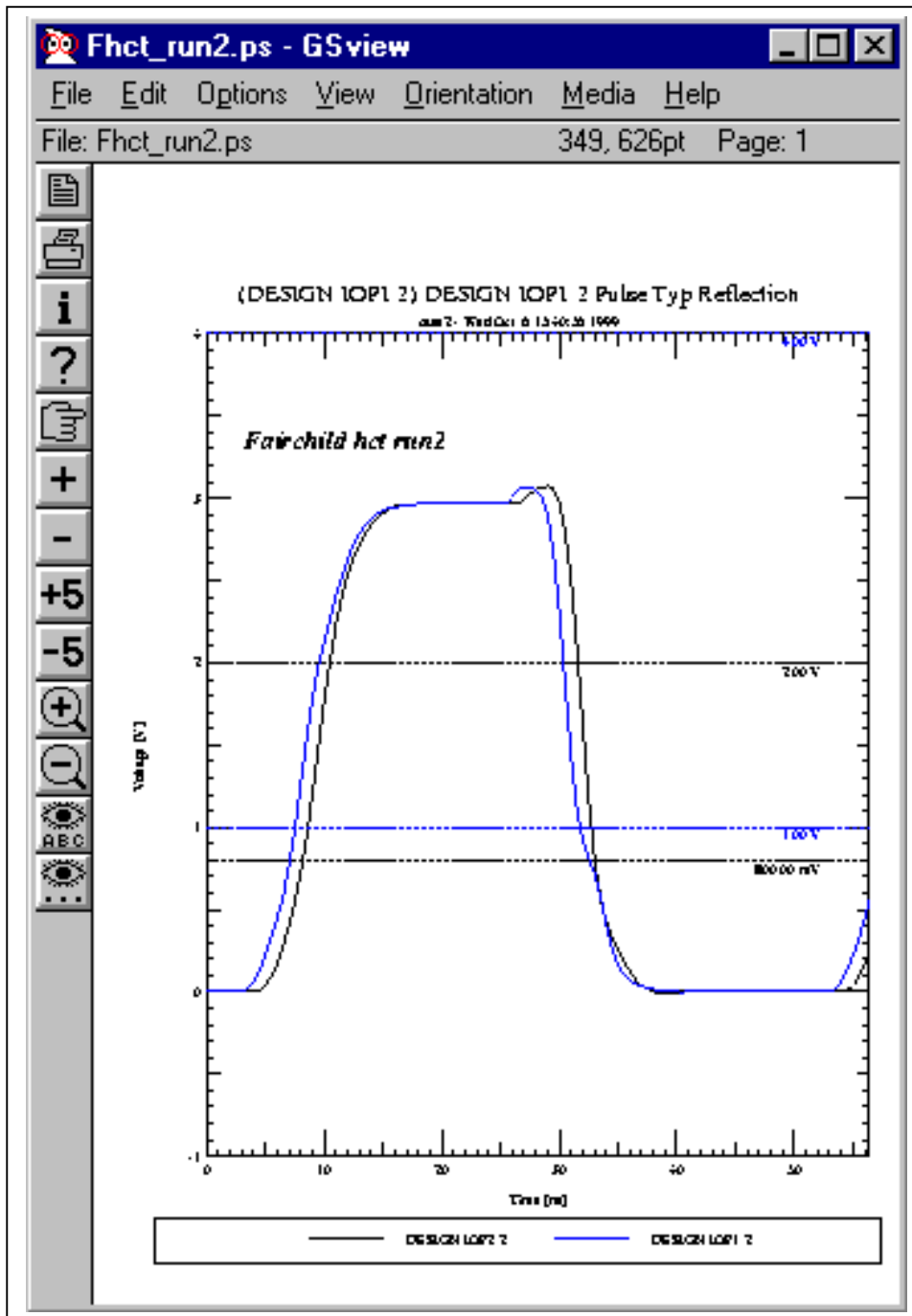
Un-Terminated



Fairchild HCT: Driver = 74HCT245SC data\_io, Receiver = 74HCT245SC data\_io  
Run1



Terminated

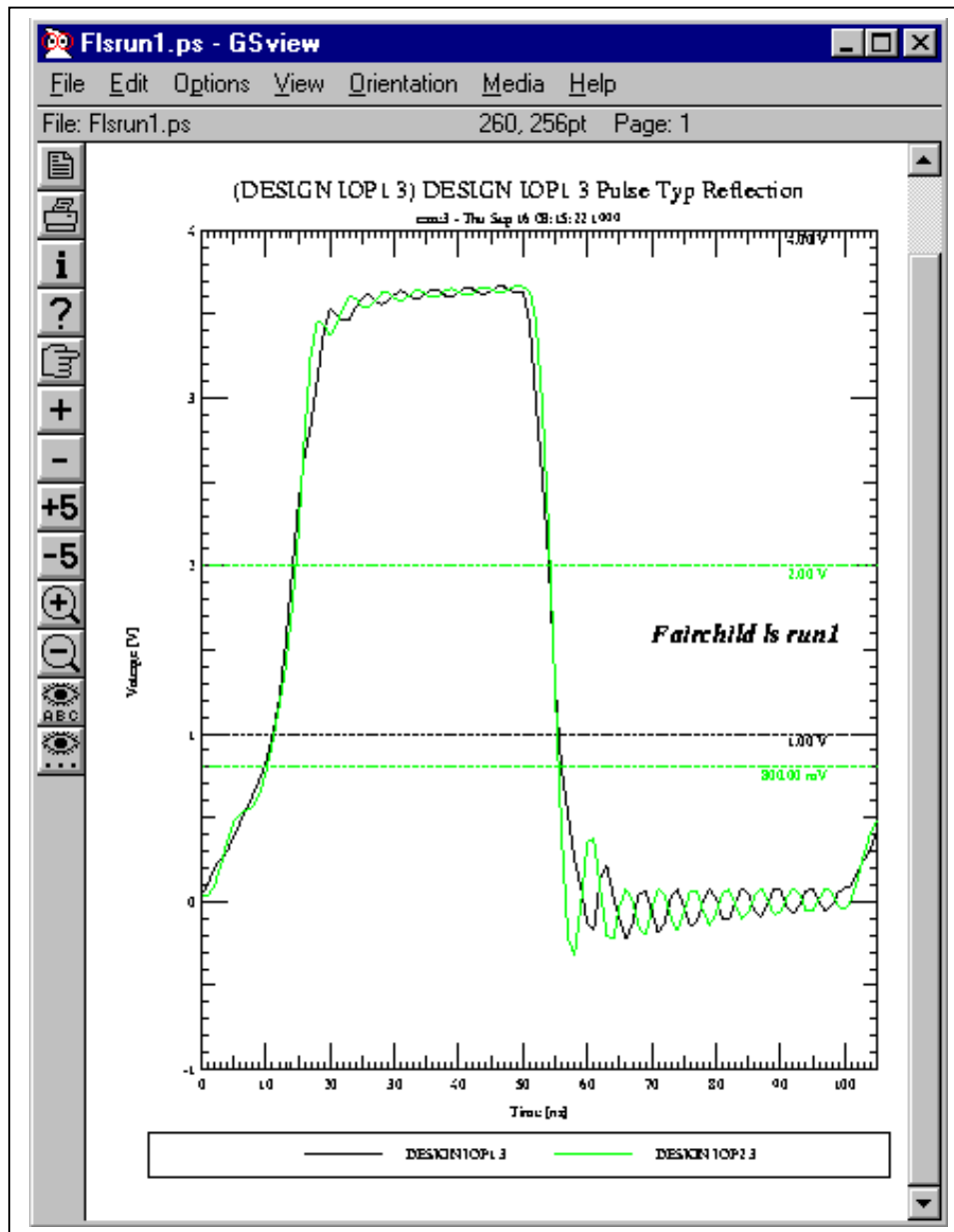


Fairchild HCT: Driver = 74HCT245SC data\_io, Receiver = 74HCT245SC data\_io  
Run2

## LS: Low Power Schottky Logic

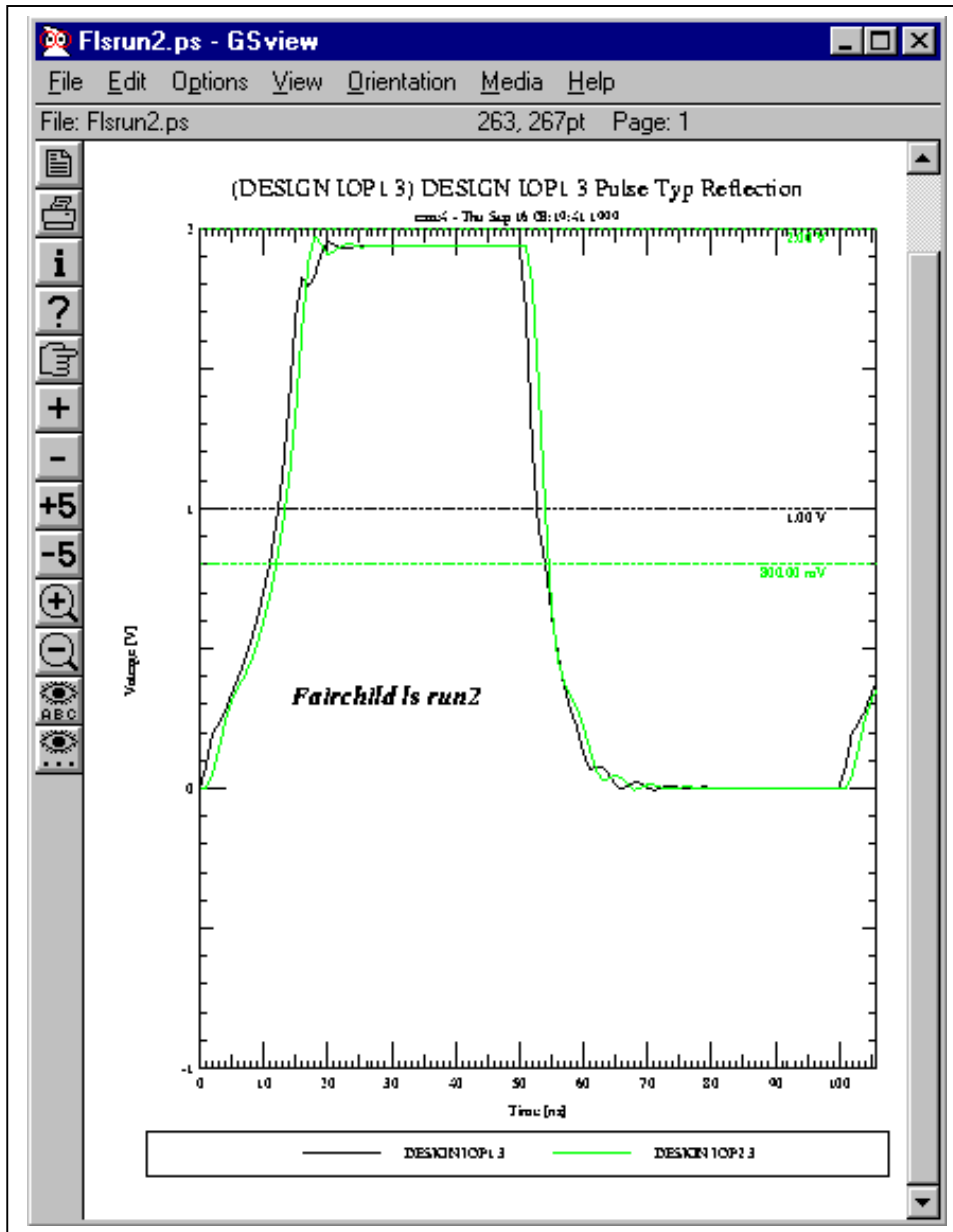
TI, Fairchild

Un-Terminated



Fairchild LS: Driver = 74LS245SC data\_io, Receiver = 74LS245SC data\_io  
Run1

Terminated



Fairchild LS: Driver = 74LS245SC data\_io, Receiver = 74LS245SC data\_io  
Run2

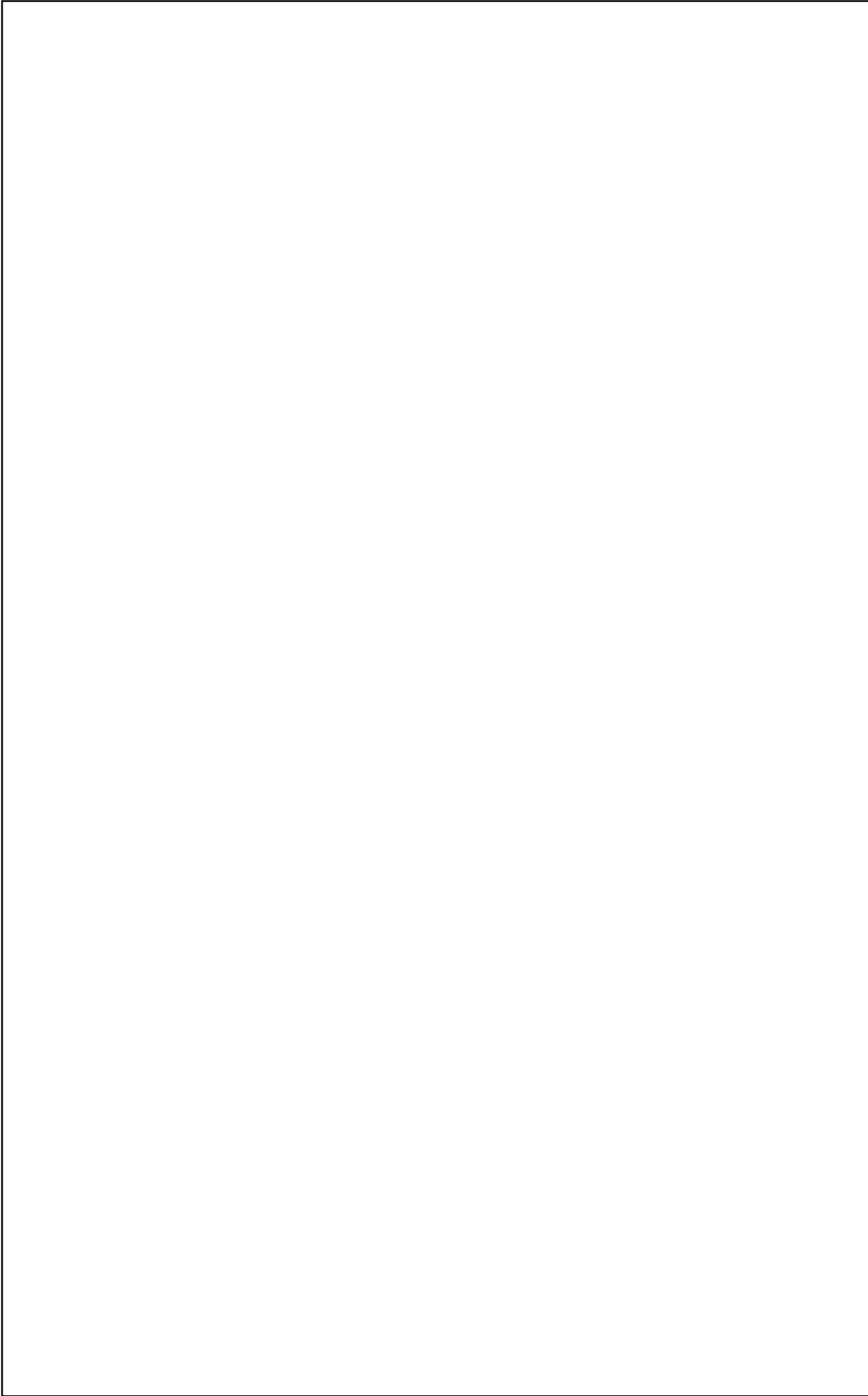
**\*S: Schottky Logic**

TI

Un-Terminated



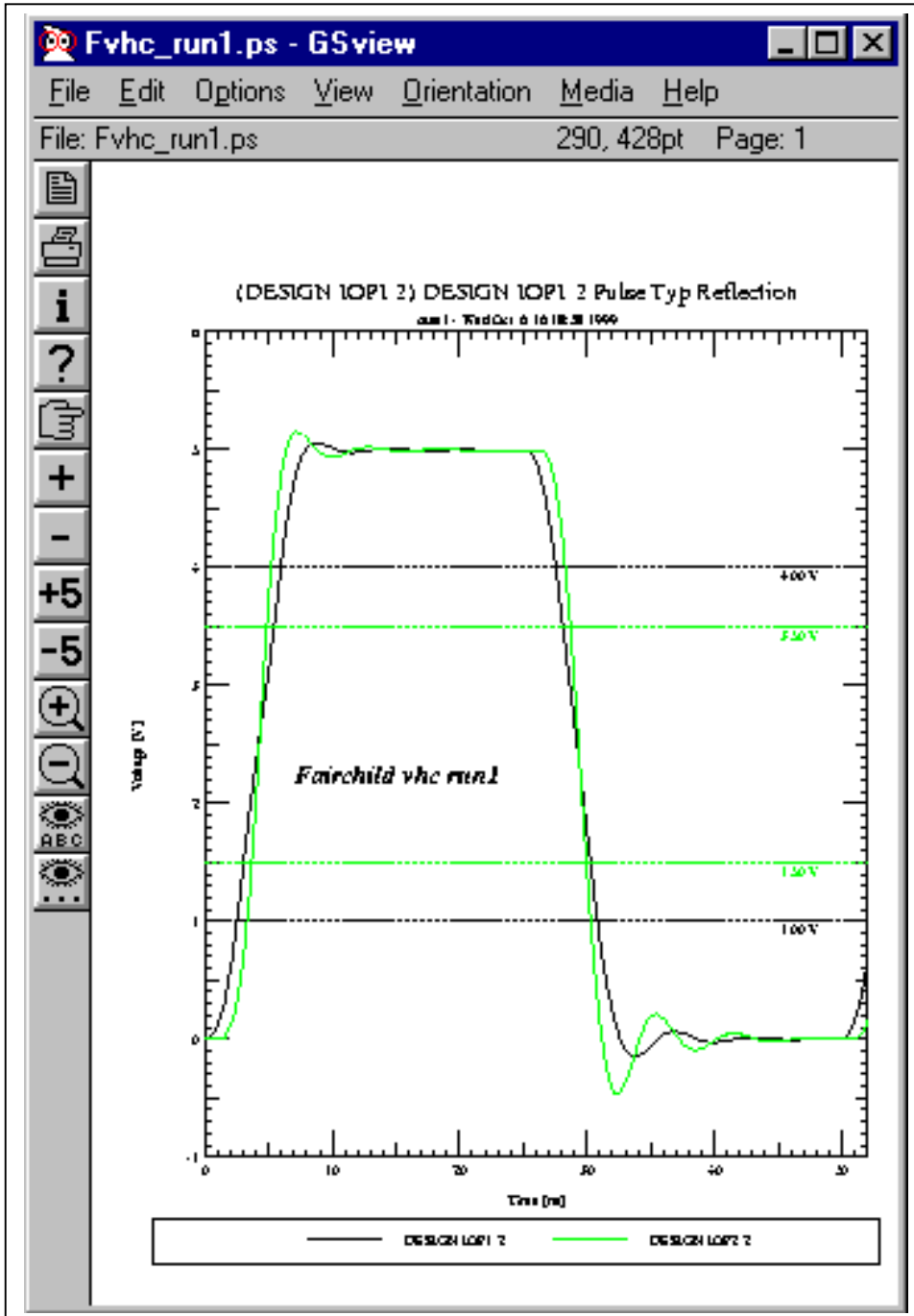
Terminated



VHC:

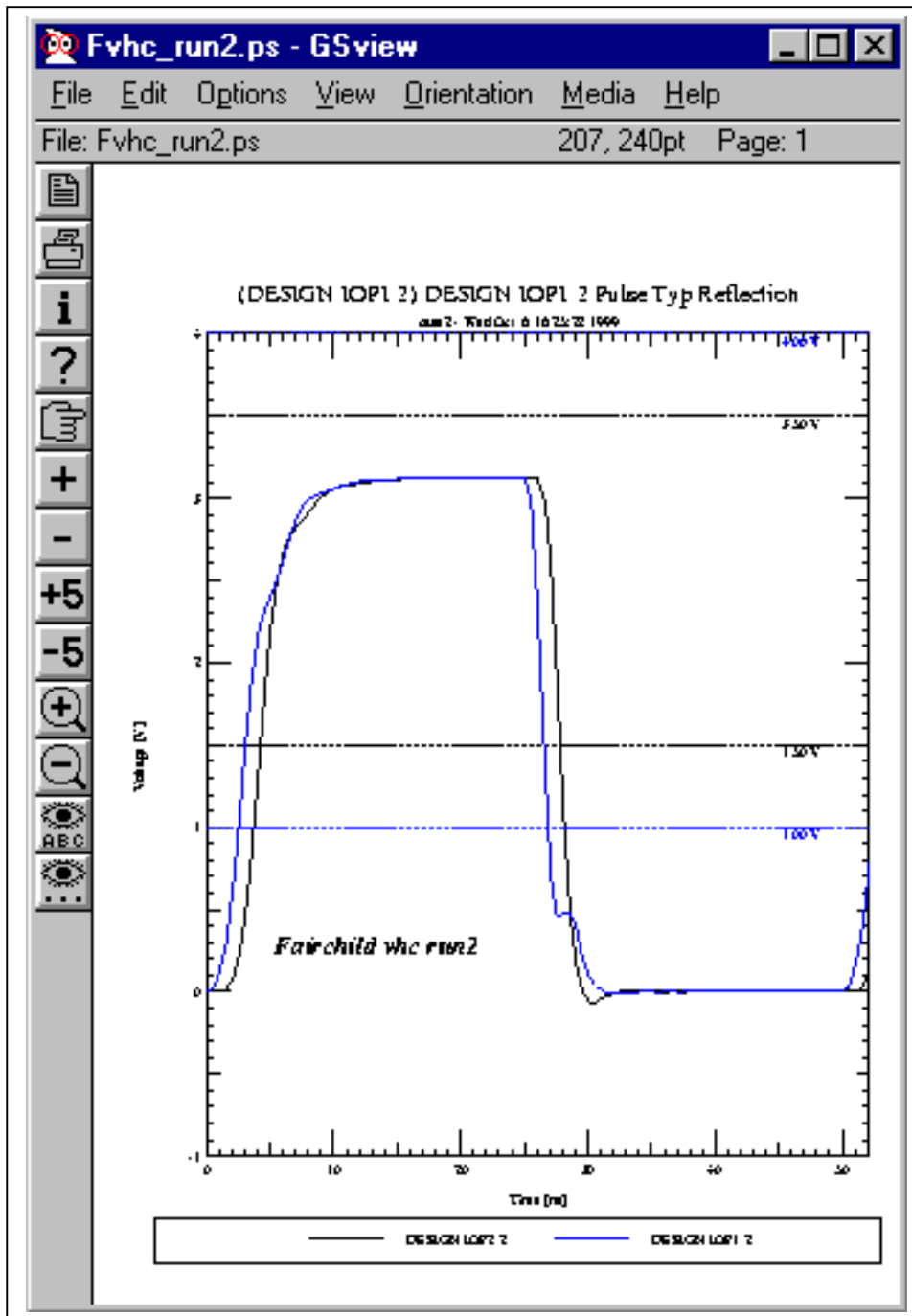
Fairchild

Un-Terminated



Fairchild VHC: Driver = 74VHC245SC data\_io, Receiver = 74VHC245SC data\_io  
Run1

Terminated



Fairchild VHC: Driver = 74VHC245SC data\_io, Receiver = 74VHC245SC data\_io  
Run2





### **3.3 Volt Logic**

CMOS: AC, ACQ, ALVC, LCX, LV, LVC, LVQ, LVX, VCX, VHC

BiCMOS: ALVT, LVT

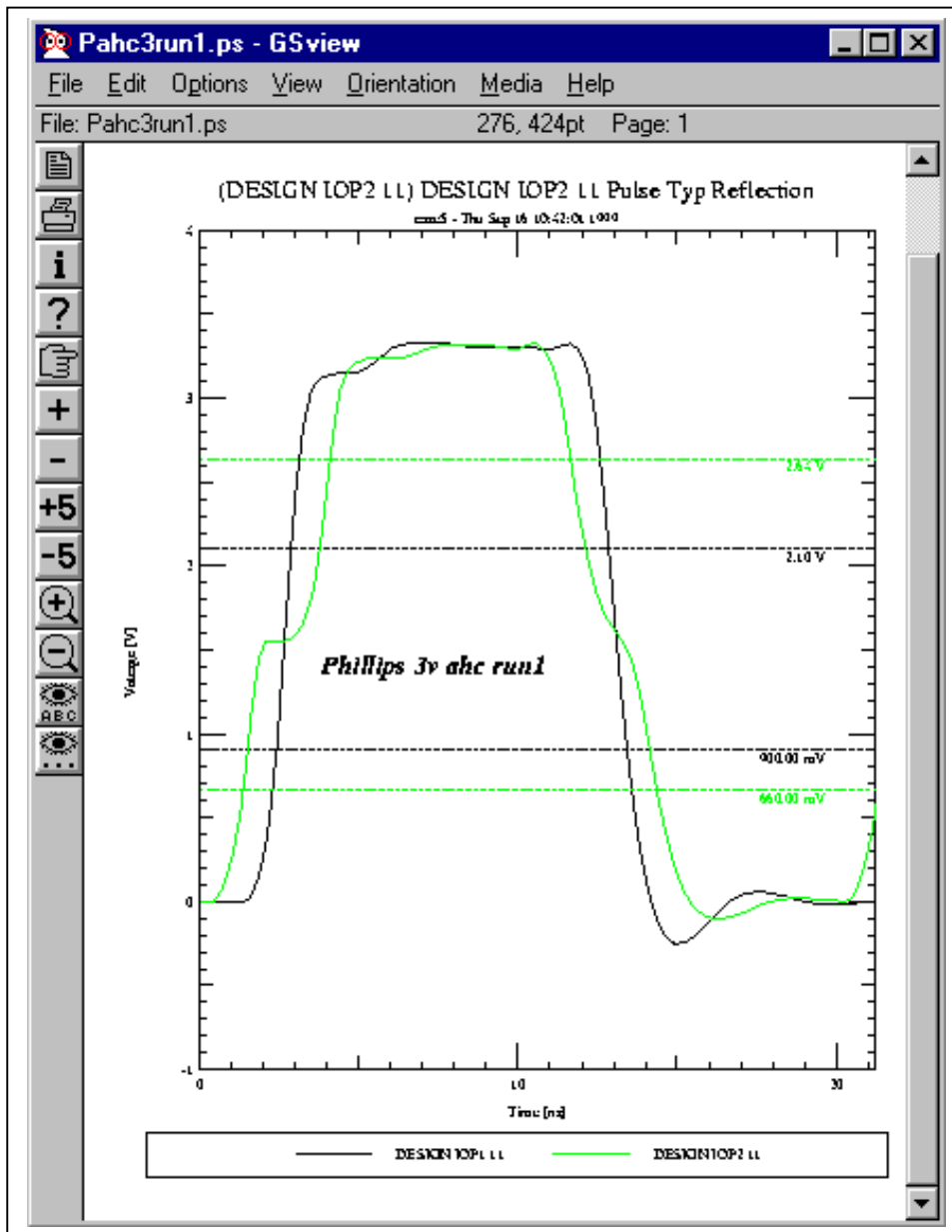
TTL (BP):

GTL, GTL+, HSTL, CTT, SSTL

## AHC/AHCT: Advanced High Speed CMOS Logic

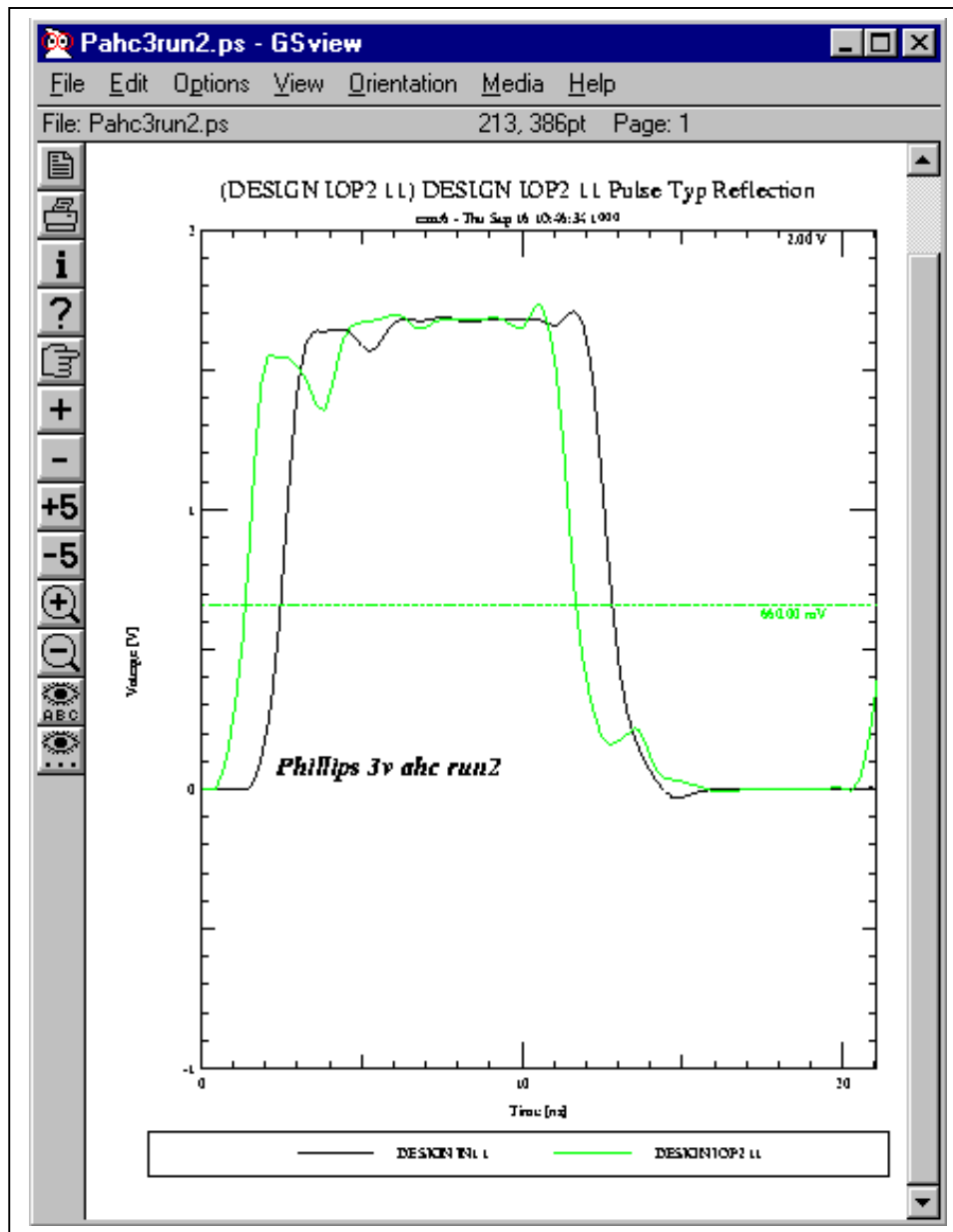
TI, Phillips

Un-Terminated



Phillips AHC: Driver = 74AHC245\_IO\_3V, Receiver = 74AHC245\_IO\_3V  
Run1

Terminated

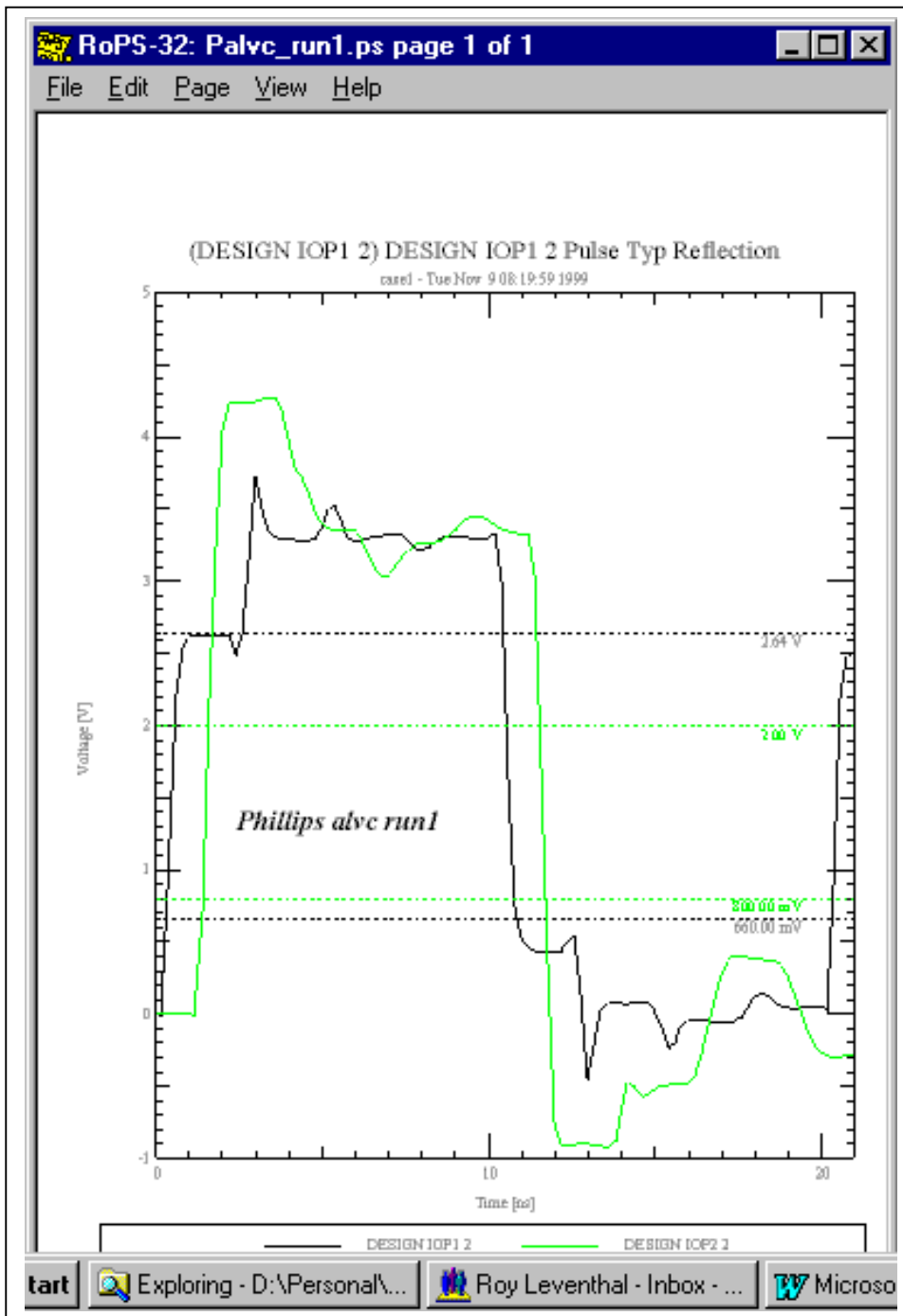


Phillips AHC: Driver = 74AHC245\_IO\_3V, Receiver = 74AHC245\_IO\_3V  
Run2

## ALVC: Advanced Low Voltage CMOS Technology

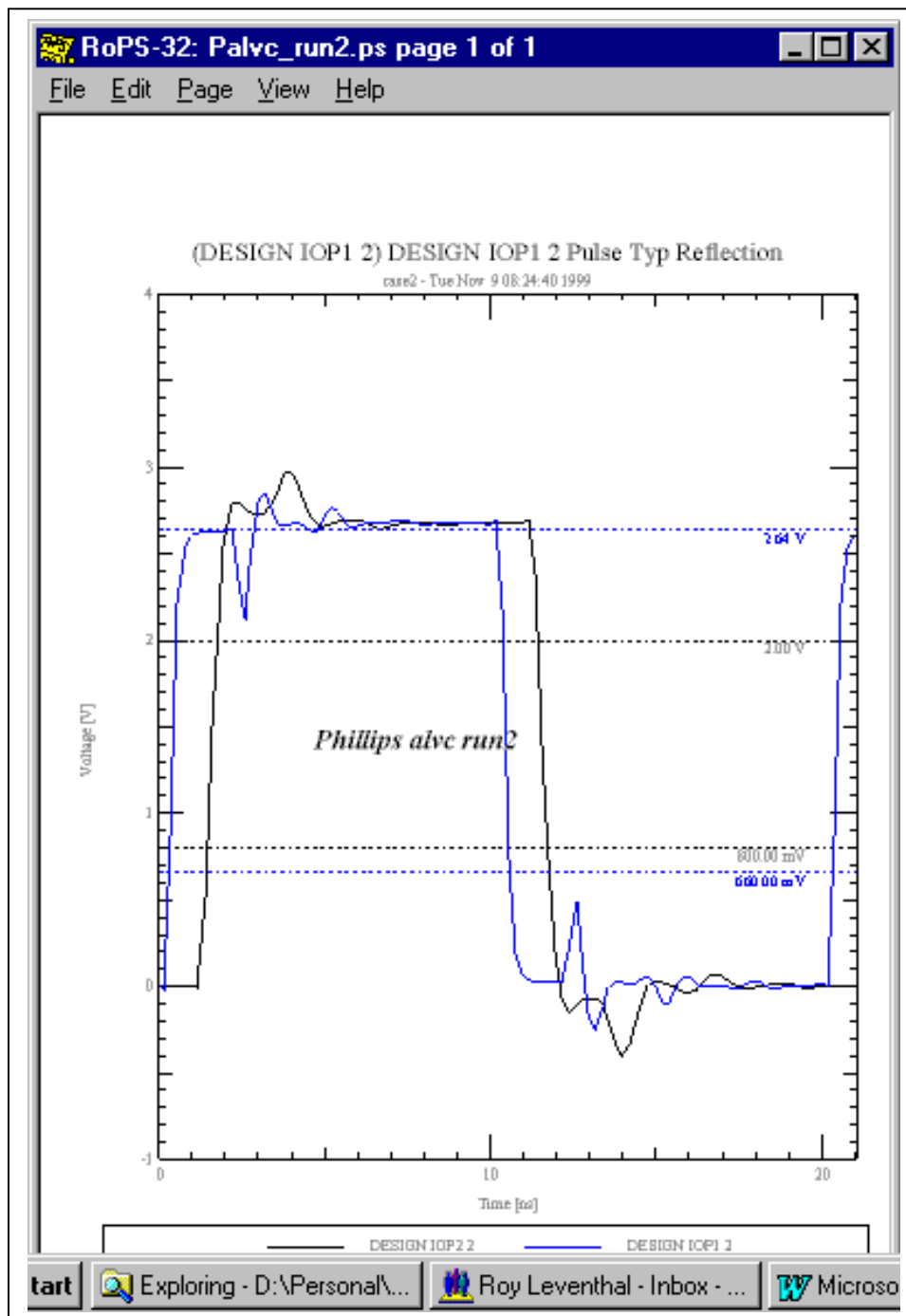
Phillips

Unterminated



Phillips ALVC: Driver = 74ALVC16245\_IO, Receiver = 74ALVC16245\_IO  
Run1

Terminated

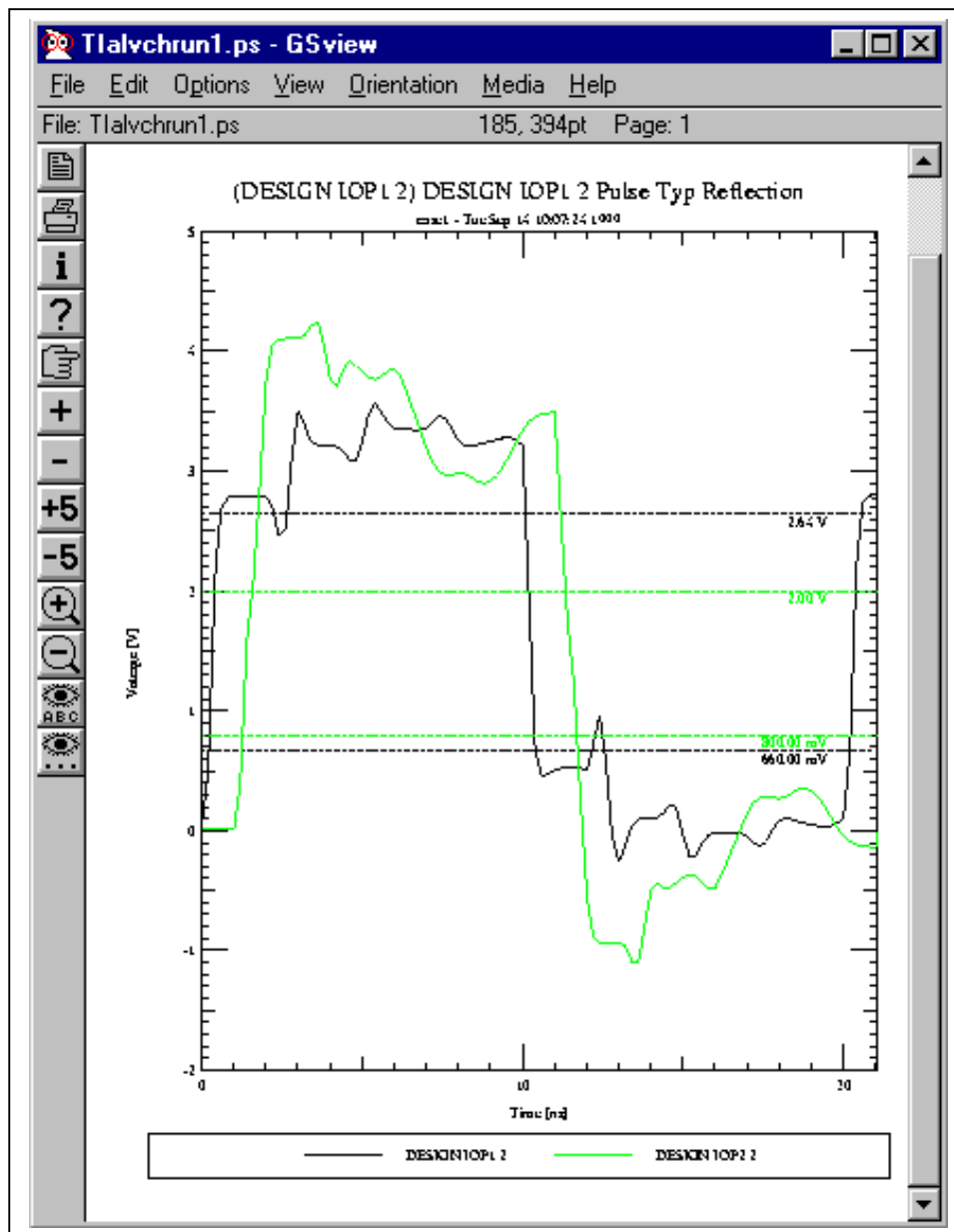


Phillips ALVC: Driver = 74ALVC16245\_IO, Receiver = 74ALVC16245\_IO  
Run2

## ALVCH: Advanced Low Voltage CMOS Technology

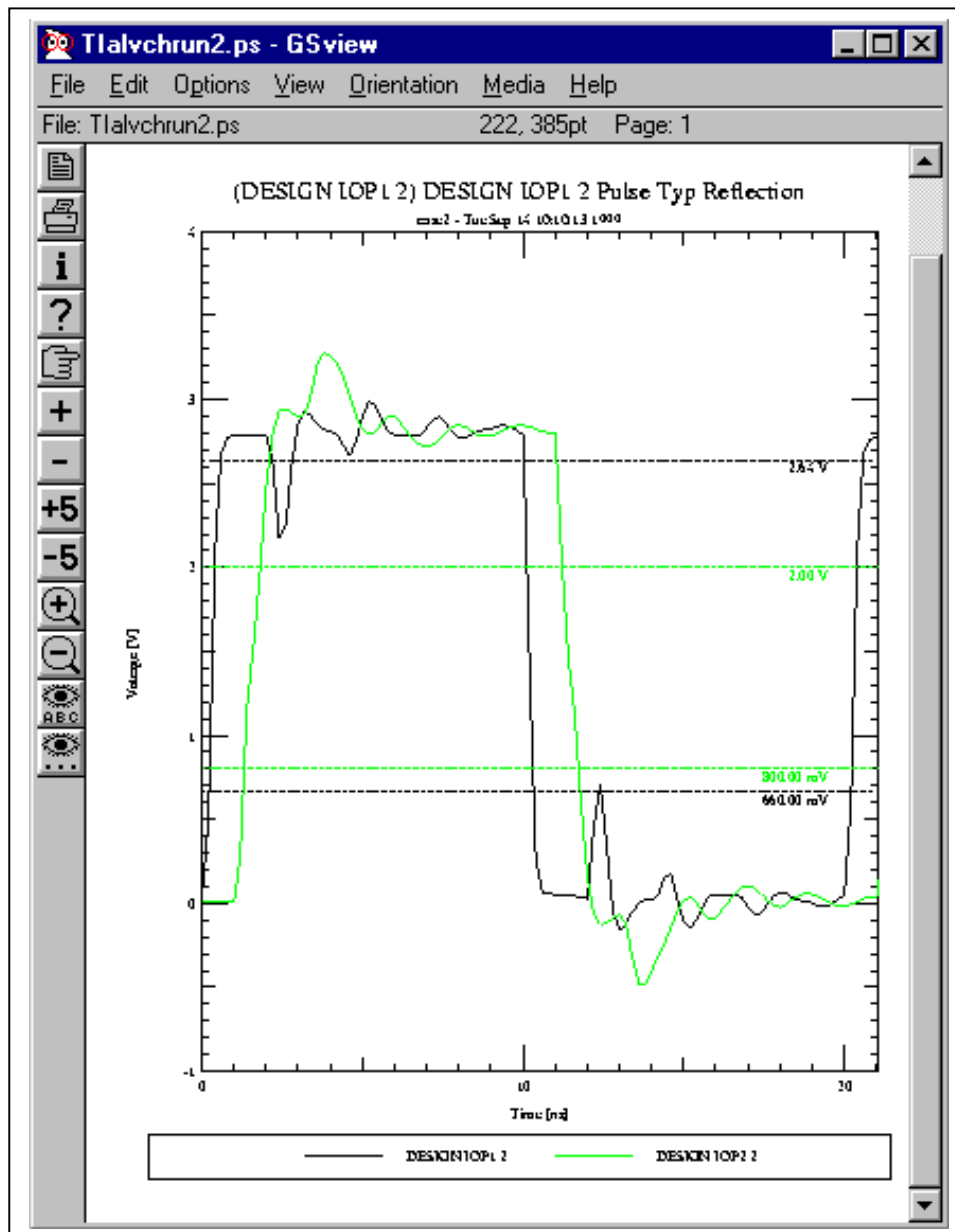
TI, Phillips

Un-Terminated

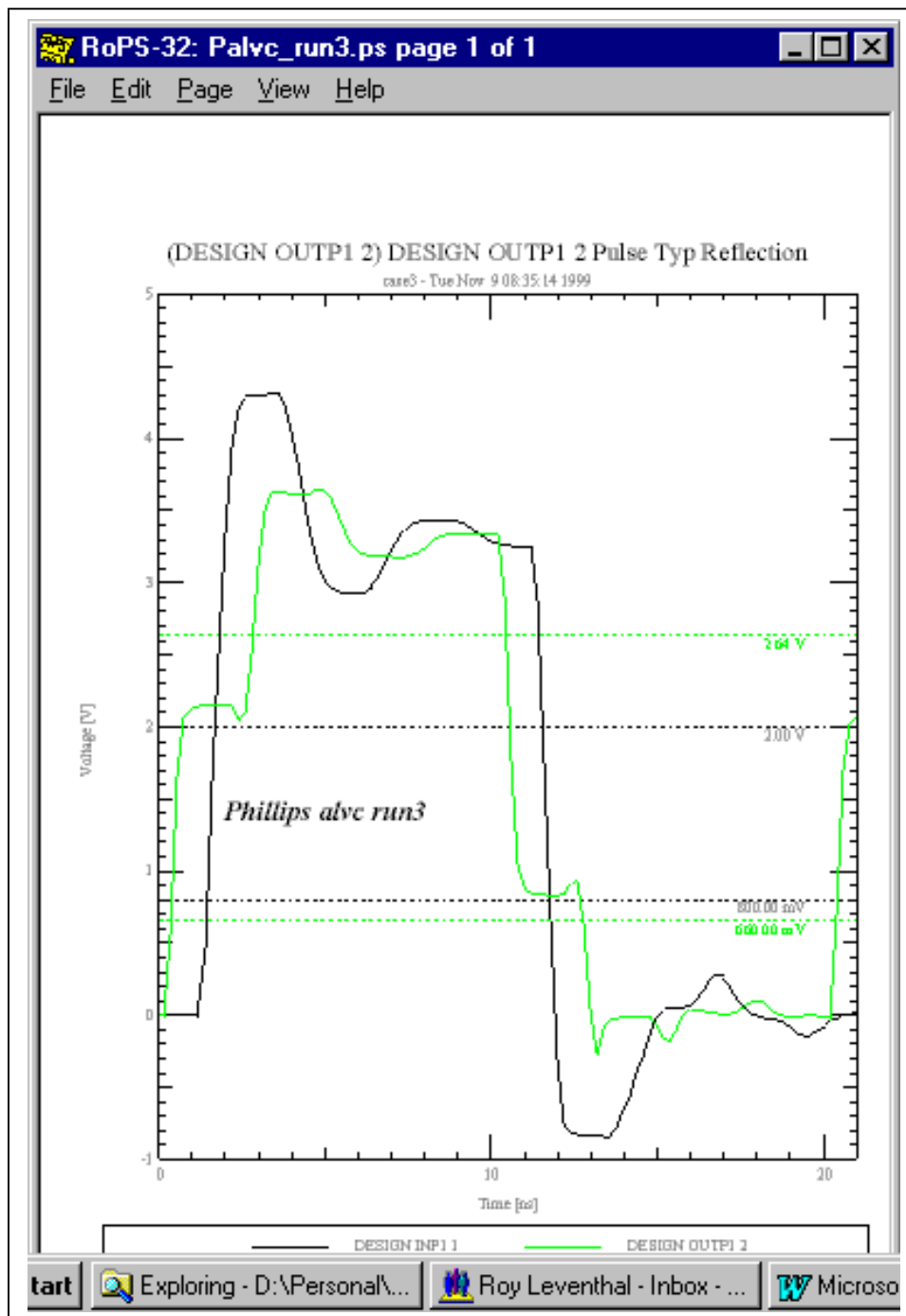


TI: Driver = ALVCH16245\_IO, Receiver =ALVCH16245\_IO  
Run1

Terminated



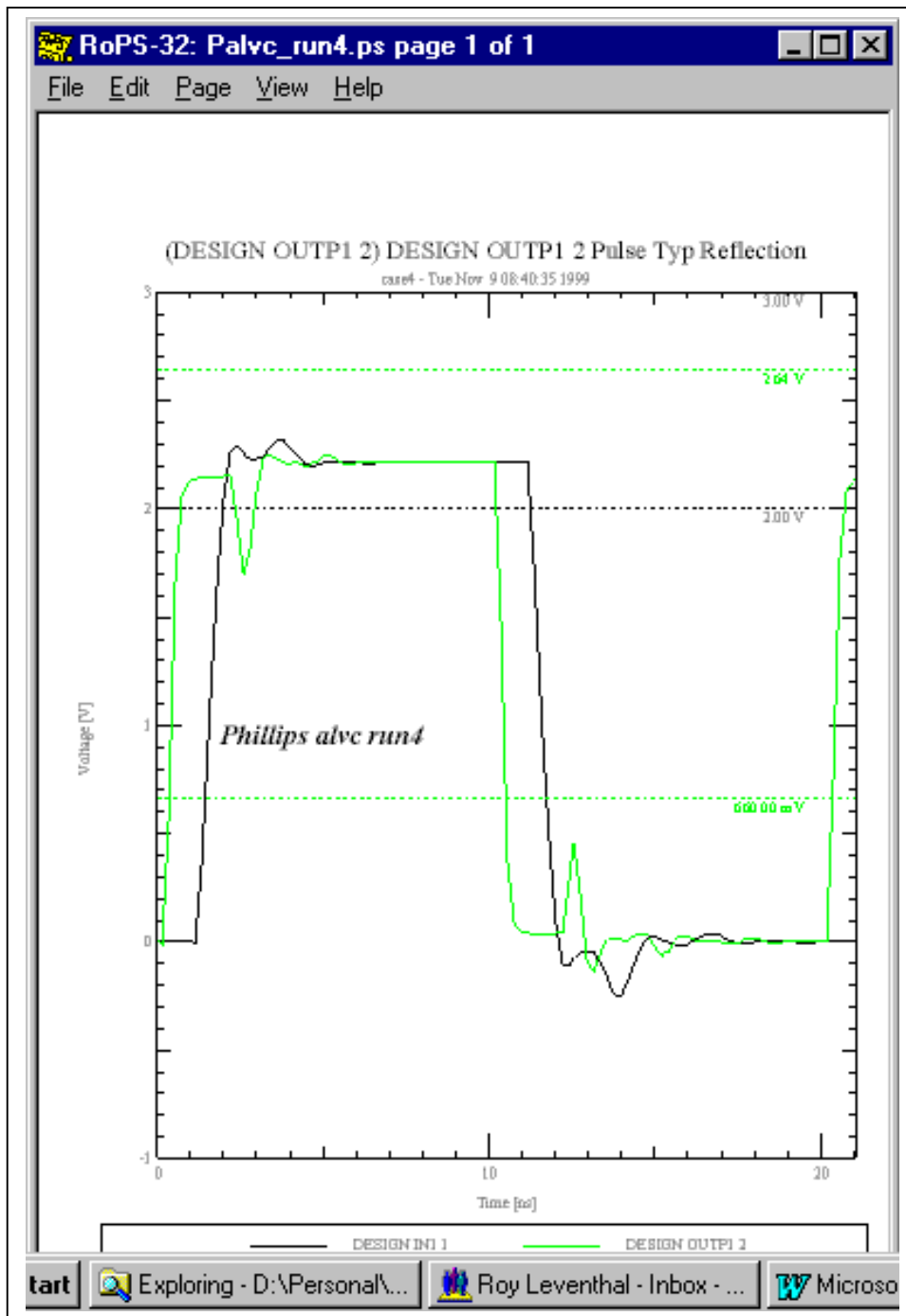
Un-Terminated



Phillips ALVCH: Driver = 74ALVCH162245\_OUT, Receiver = 74ALVCH162245\_IN  
Run3

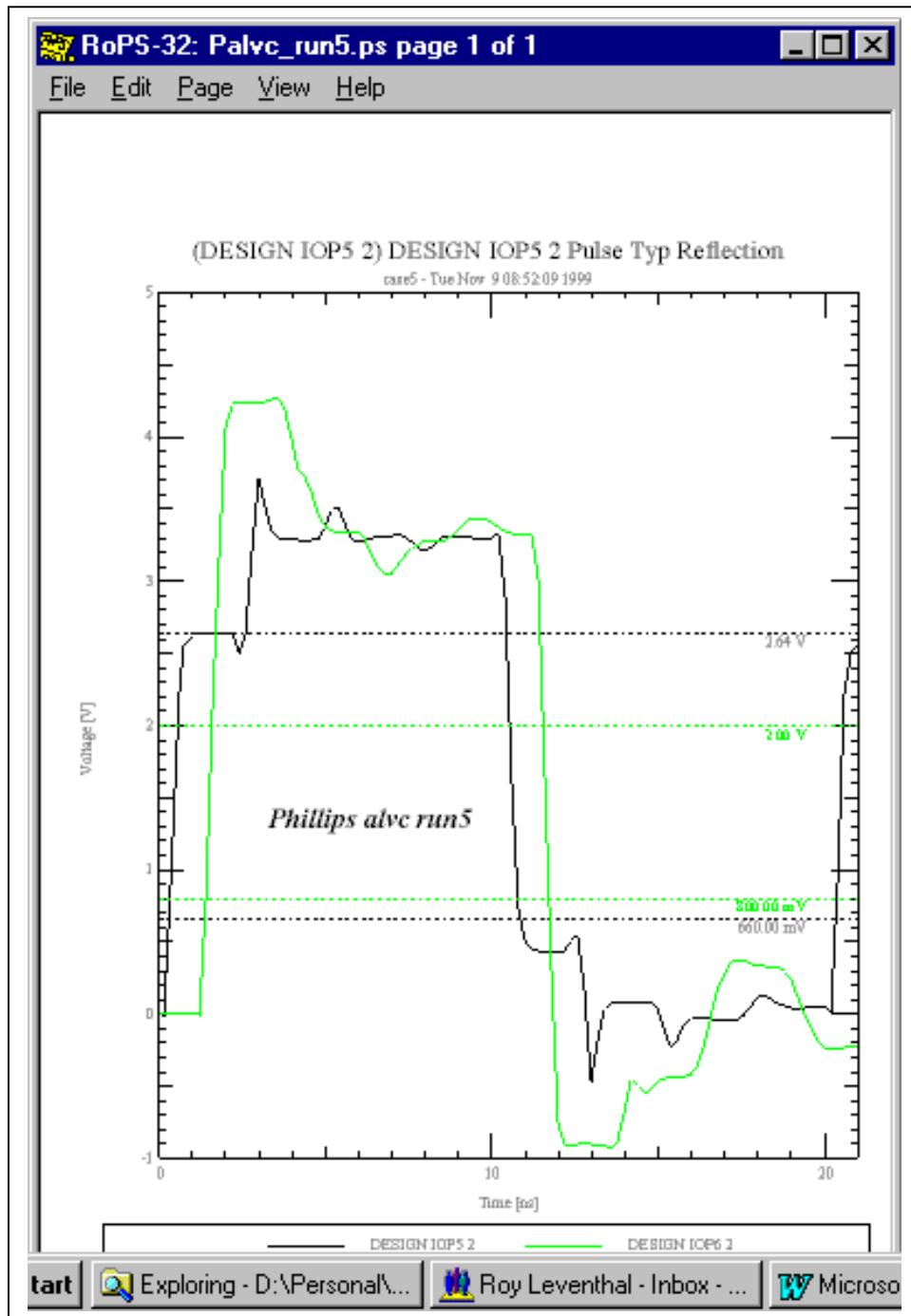


Terminated



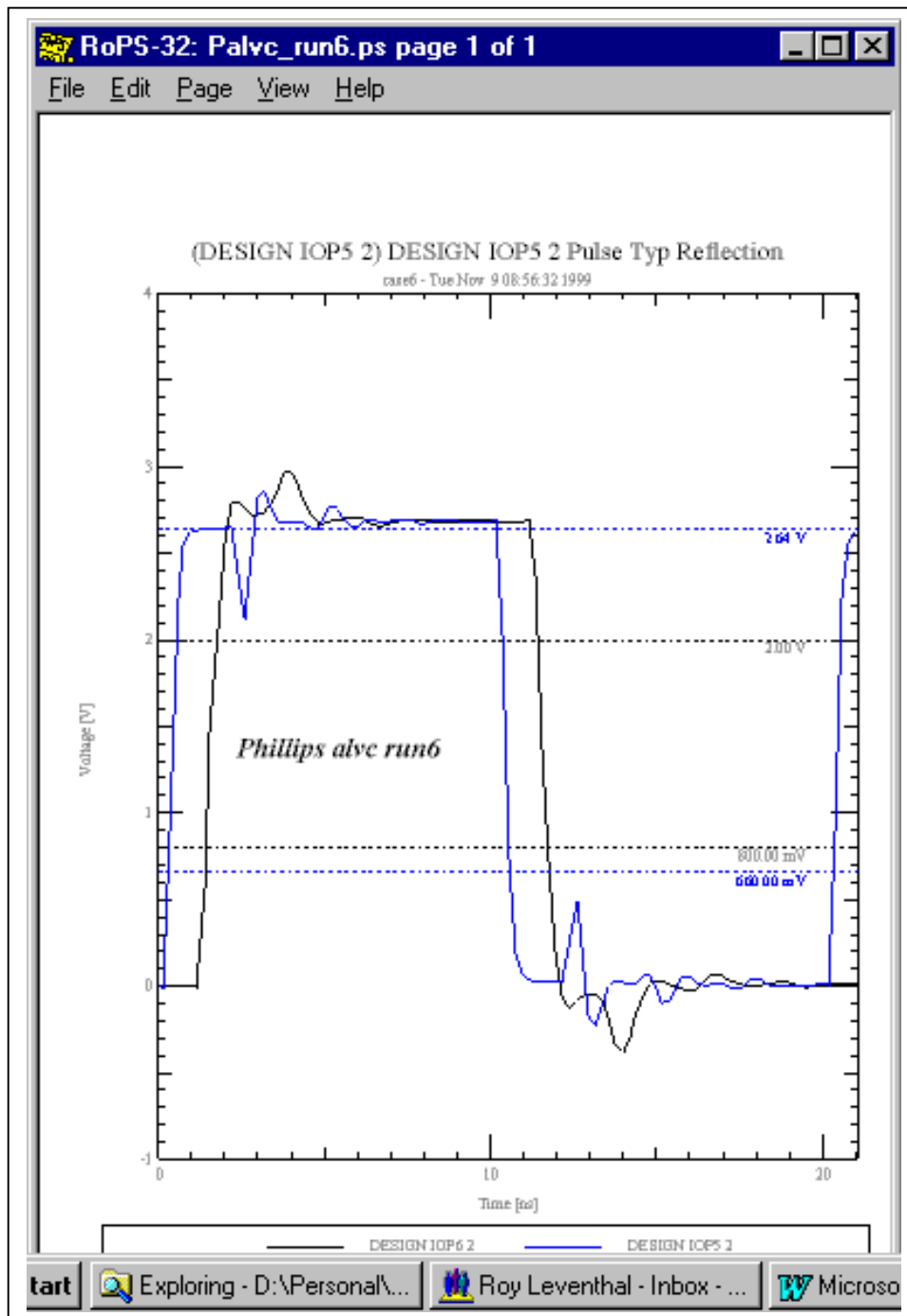
Phillips ALVCH: Driver = 74ALVCH162245\_OUT, Receiver = 74ALVCH162245\_IN  
Run4

Un-Terminated



Phillips ALVCH: Driver = 74ALVCH16245\_IO, Receiver = 74ALVCH16245\_IO  
Run5

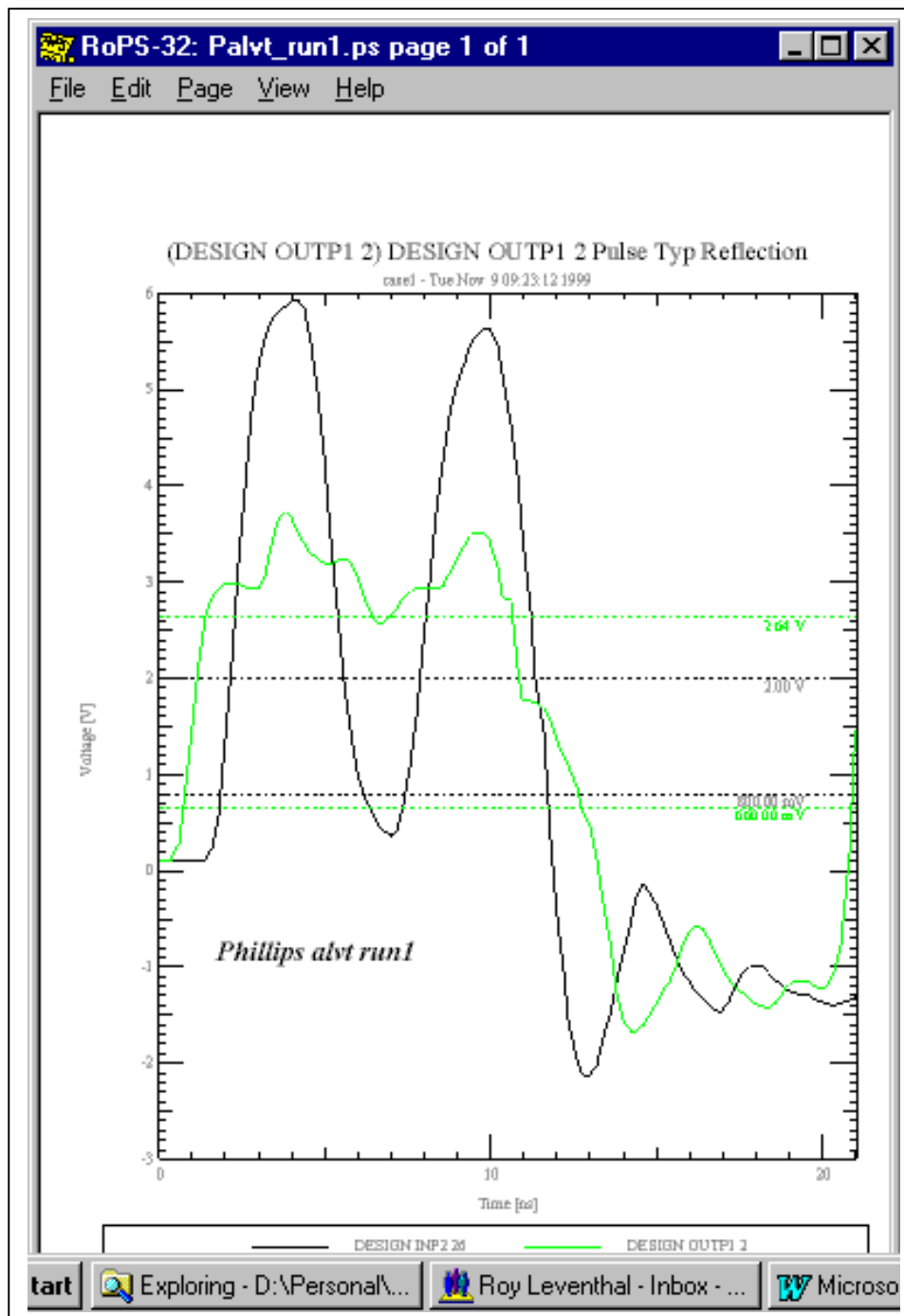
Terminated



Phillips ALVCH: Driver = 74ALVCH16245\_IO, Receiver = 74ALVCH16245\_IO  
Run6

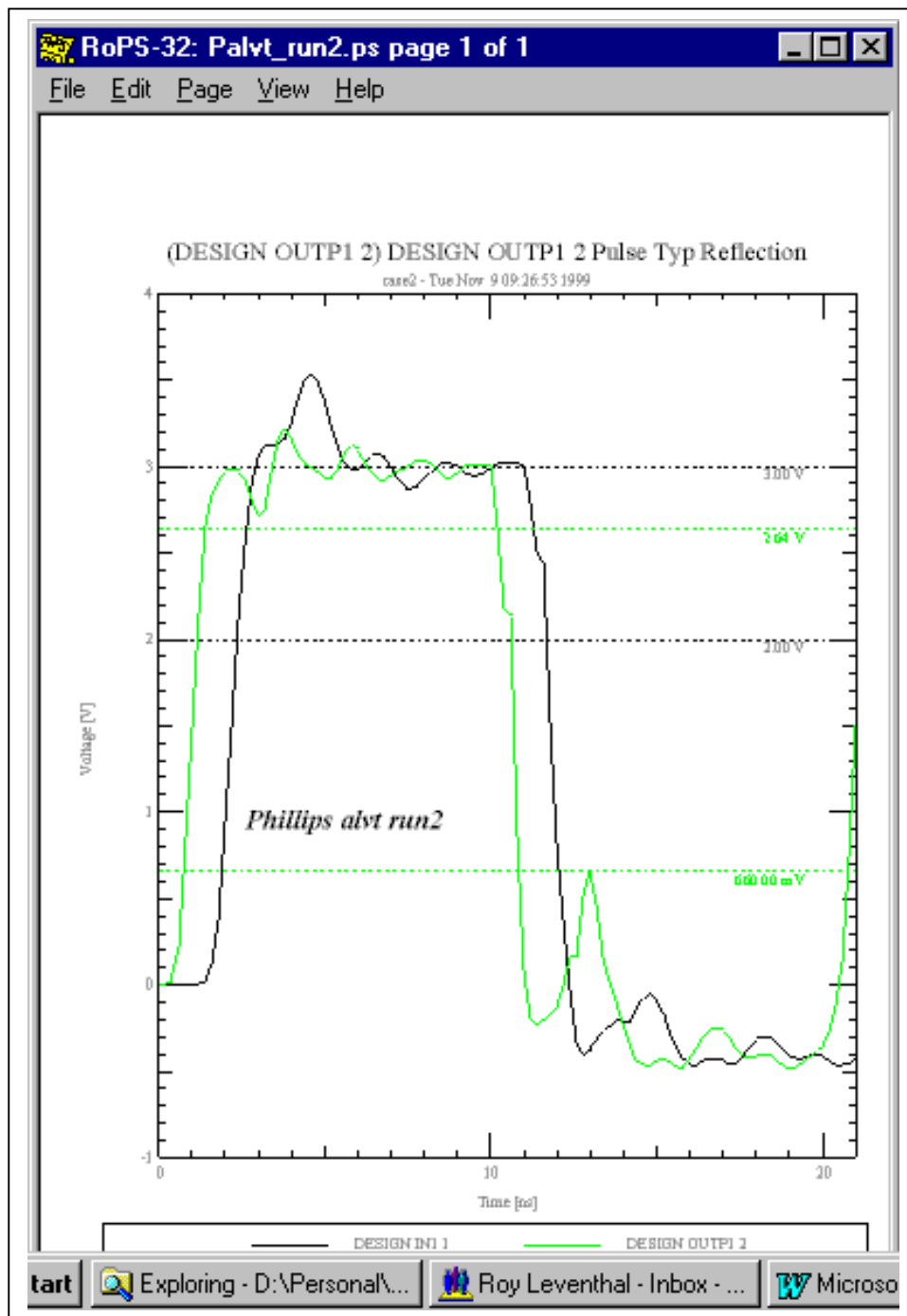
Phillips

## Un-Terminated



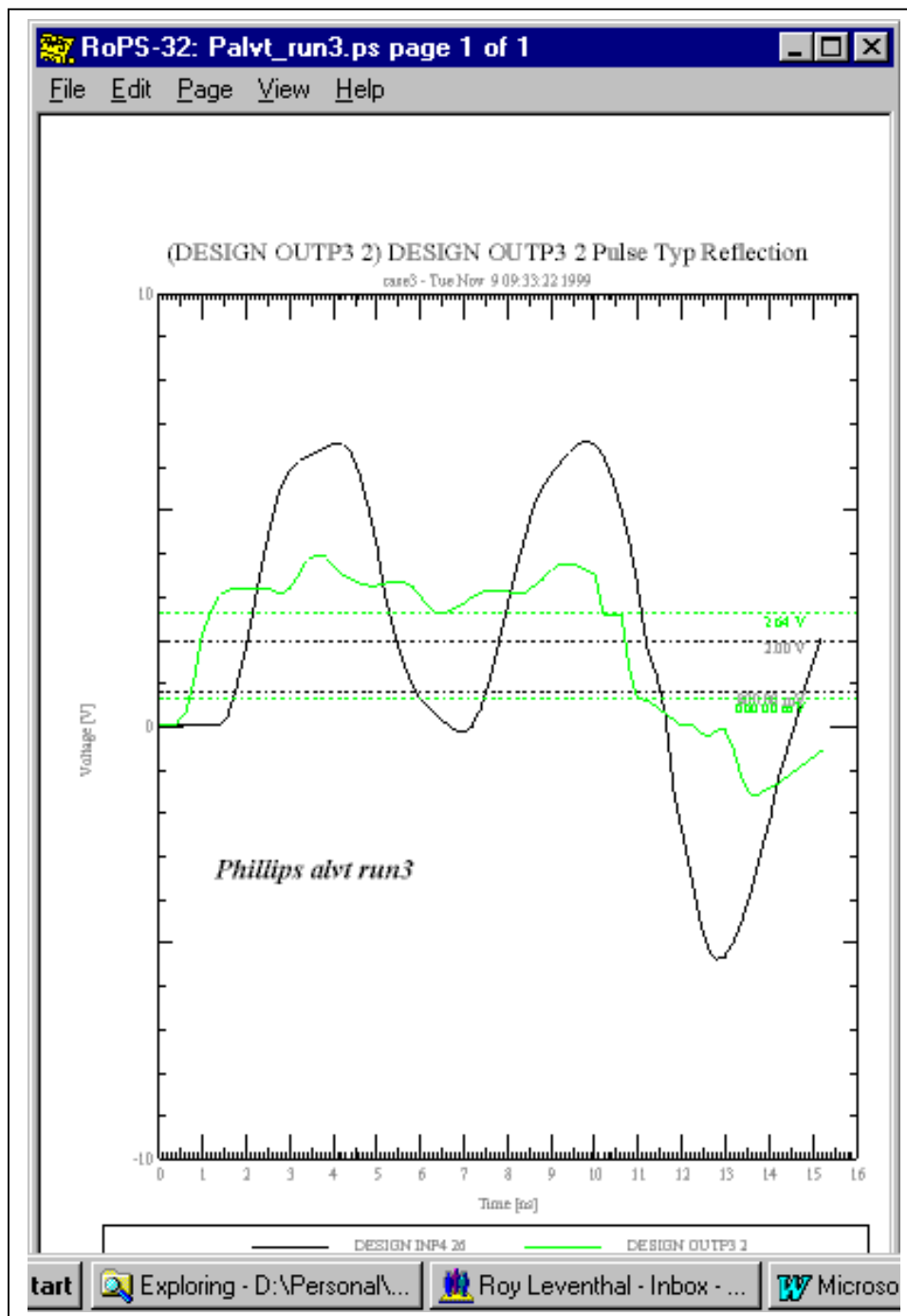
Phillips ALVT: Driver = 74ALVT162245\_OUT, Receiver = 74ALVT162245\_IN  
Run1

Terminated



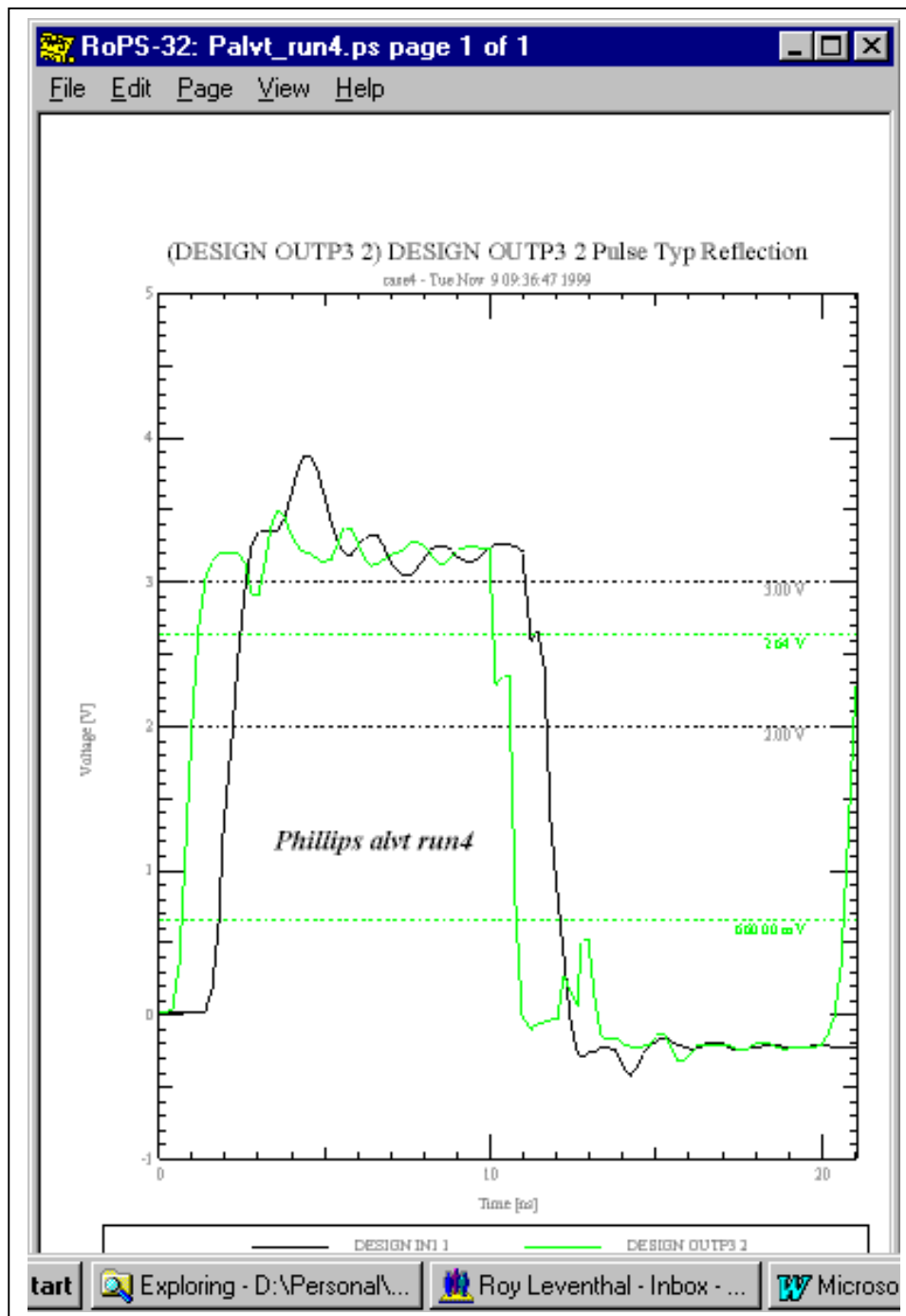
Phillips ALVT: Driver = 74ALVT162245\_OUT, Receiver = 74ALVT162245\_IN  
Run2

Unterminated



Phillips ALVT: Driver = 74ALVT16245\_OUT, Receiver = 74ALVT16245\_IN  
Run3

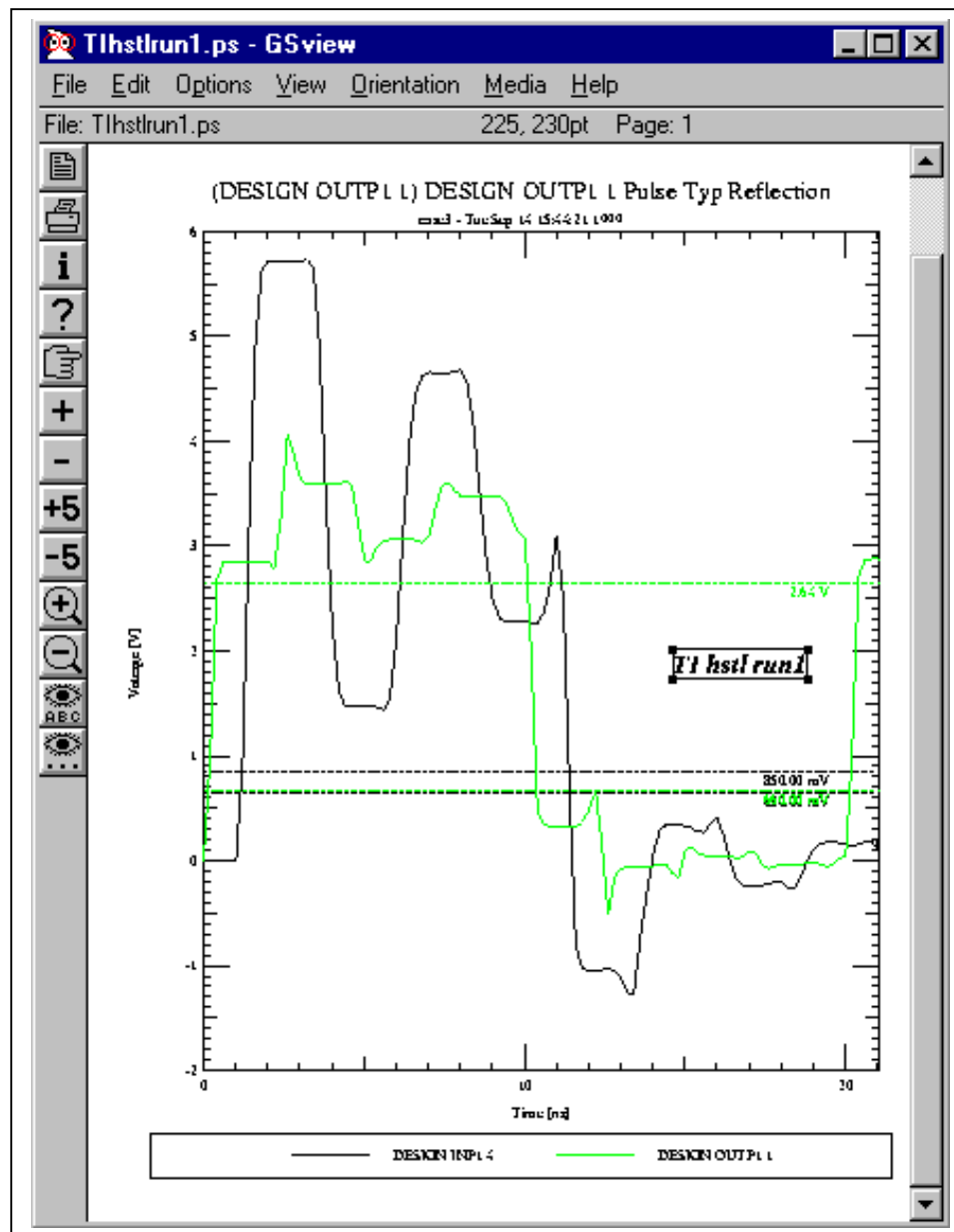
Terminated



Phillips ALVT: Driver = 74ALVT162245\_OUT, Receiver = 74ALVT162245\_IN  
Run2

TI

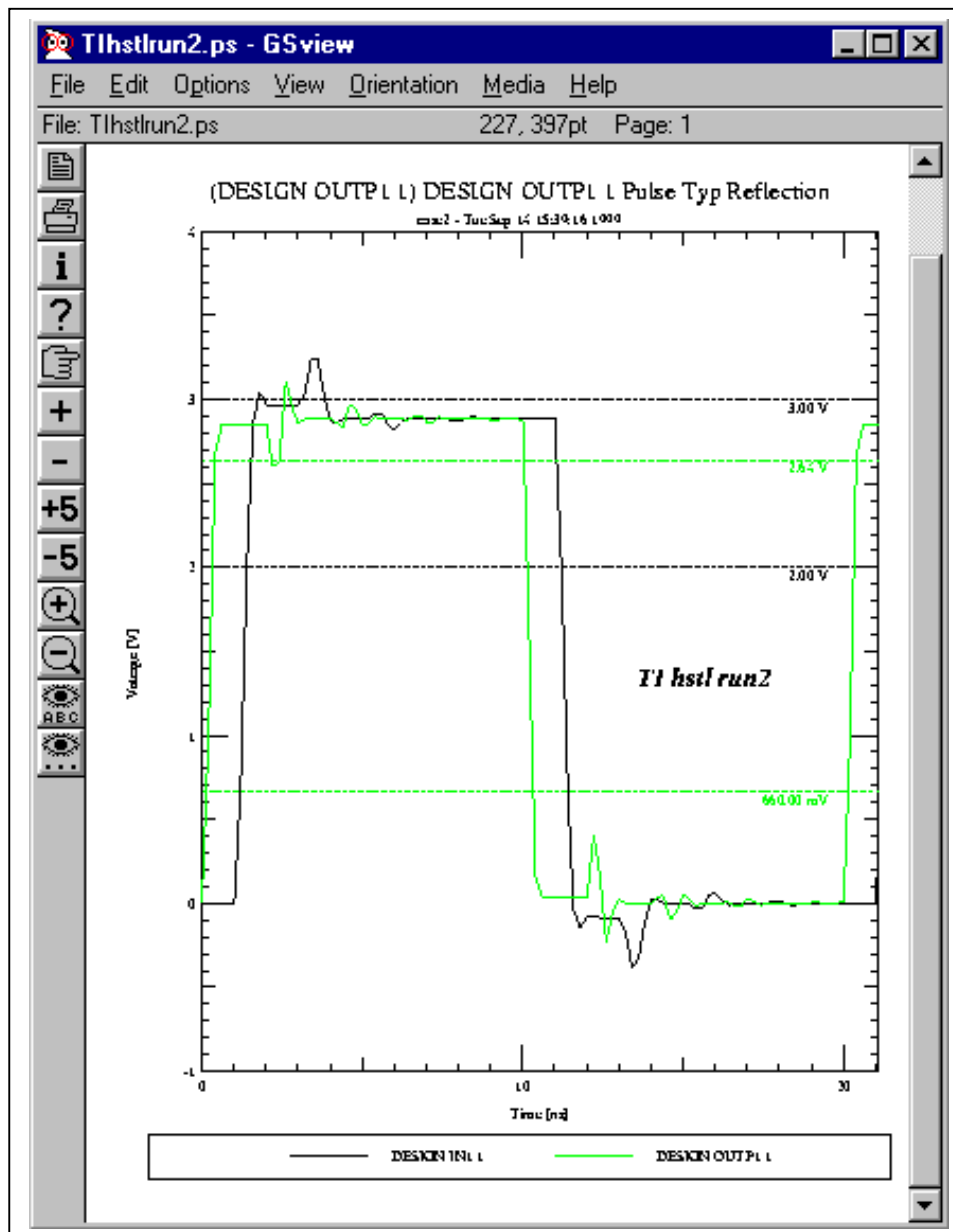
Un-Terminated



TI: Driver = HSTL16918\_OUT, Receiver = HSTL16918\_IN  
Run1



Terminated

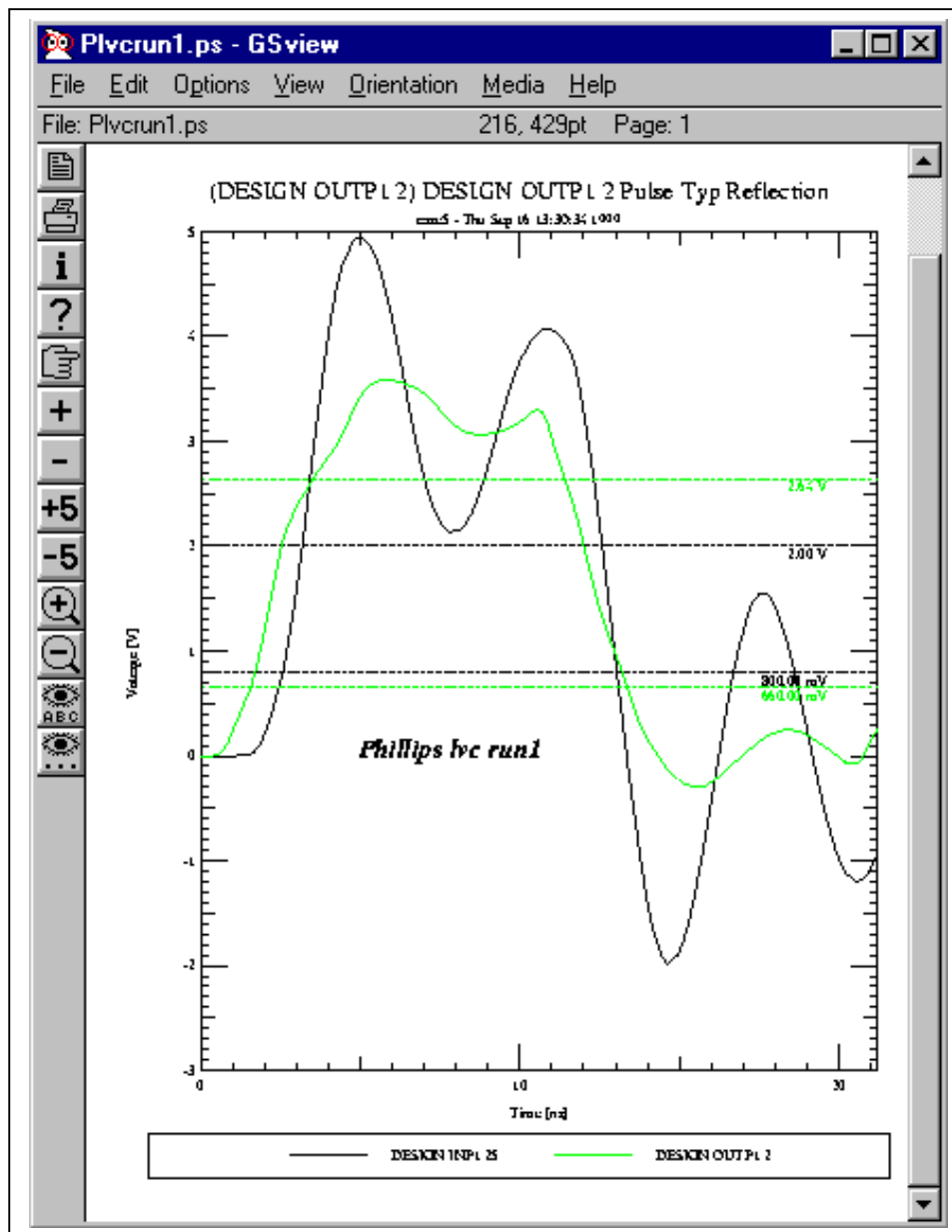


TI: Driver = HSTL16918\_OUT, Receiver = HSTL16918\_IN  
Run2

## LV/LVC: Low Voltage CMOS Logic

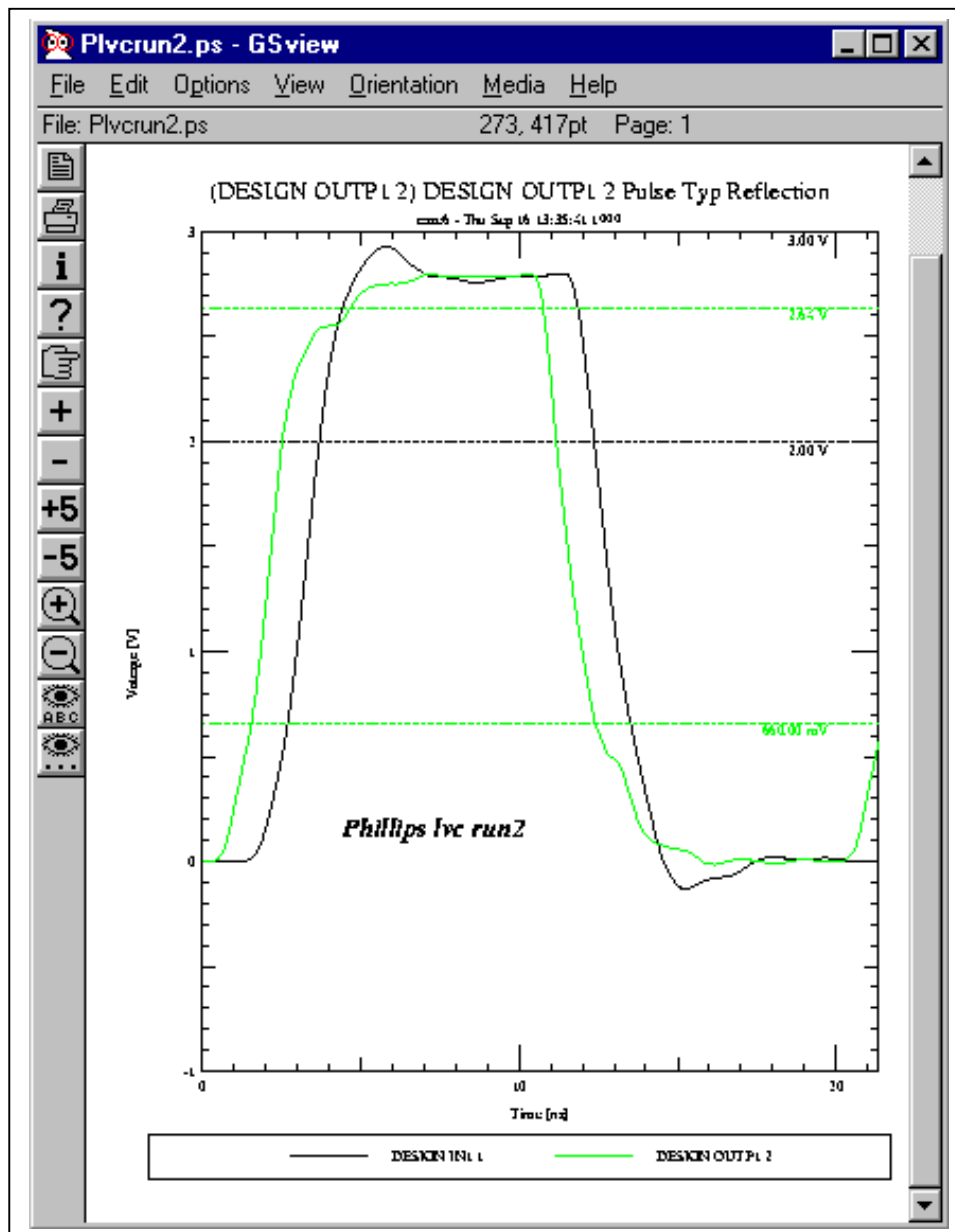
Fairchild, Phillips, TI

Un-Terminated



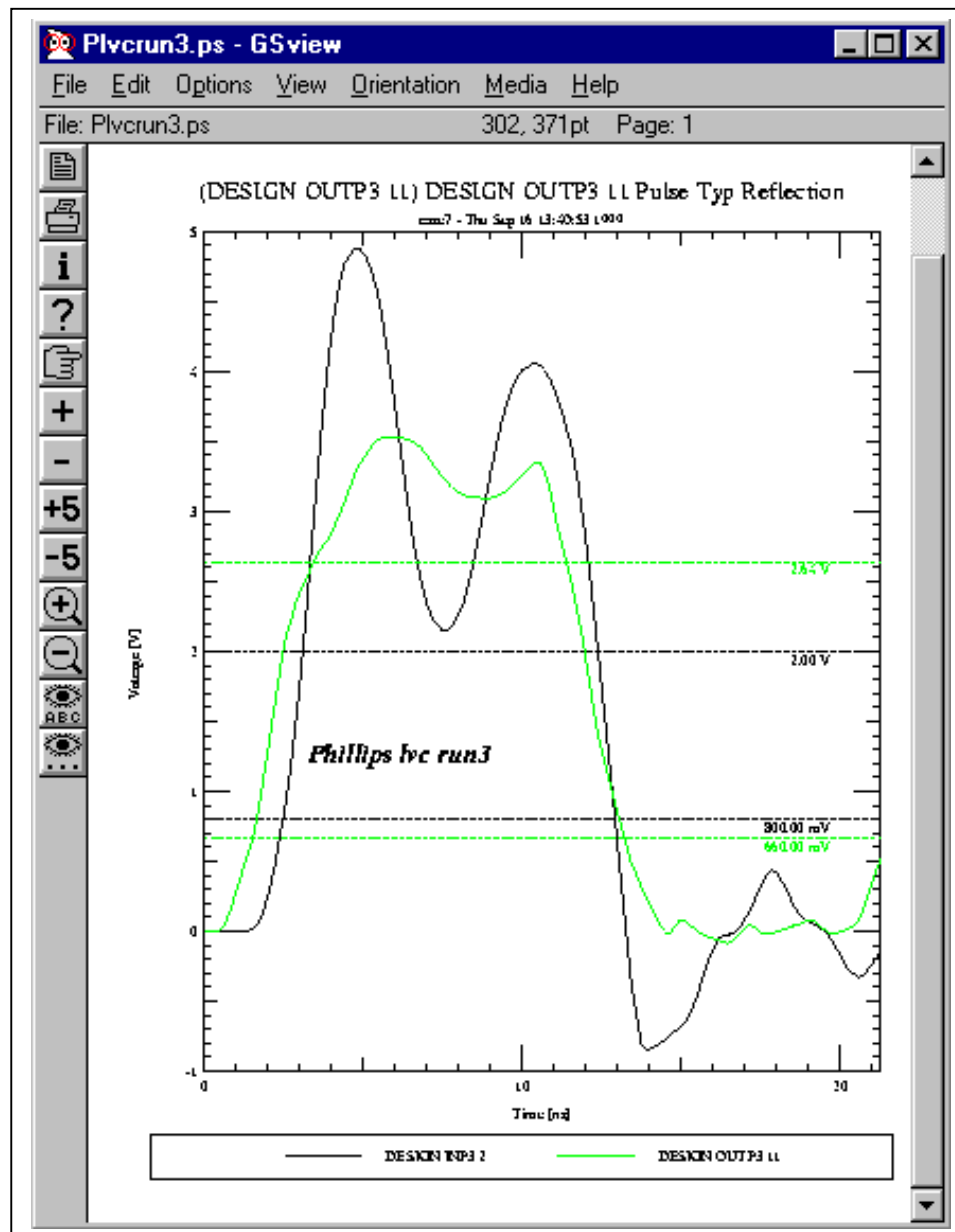
Phillips: Driver = 74LVC16245\_OUT, Receiver = 74LVC16245\_OUT  
Run1

Terminated



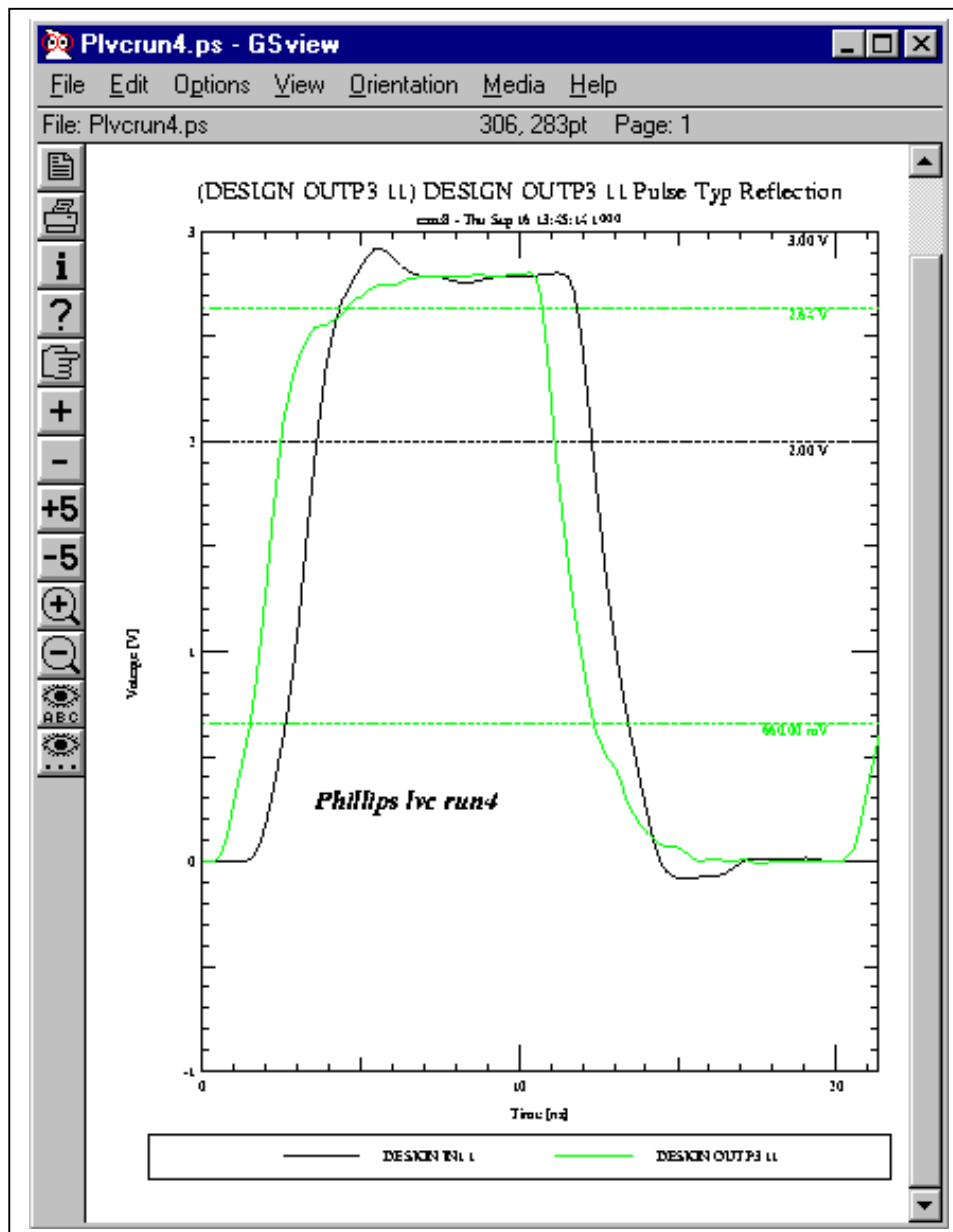
Phillips: Driver = 74LVC16245\_OUT, Receiver = 74LVC16245\_OUT  
Run2

## Un-Terminated



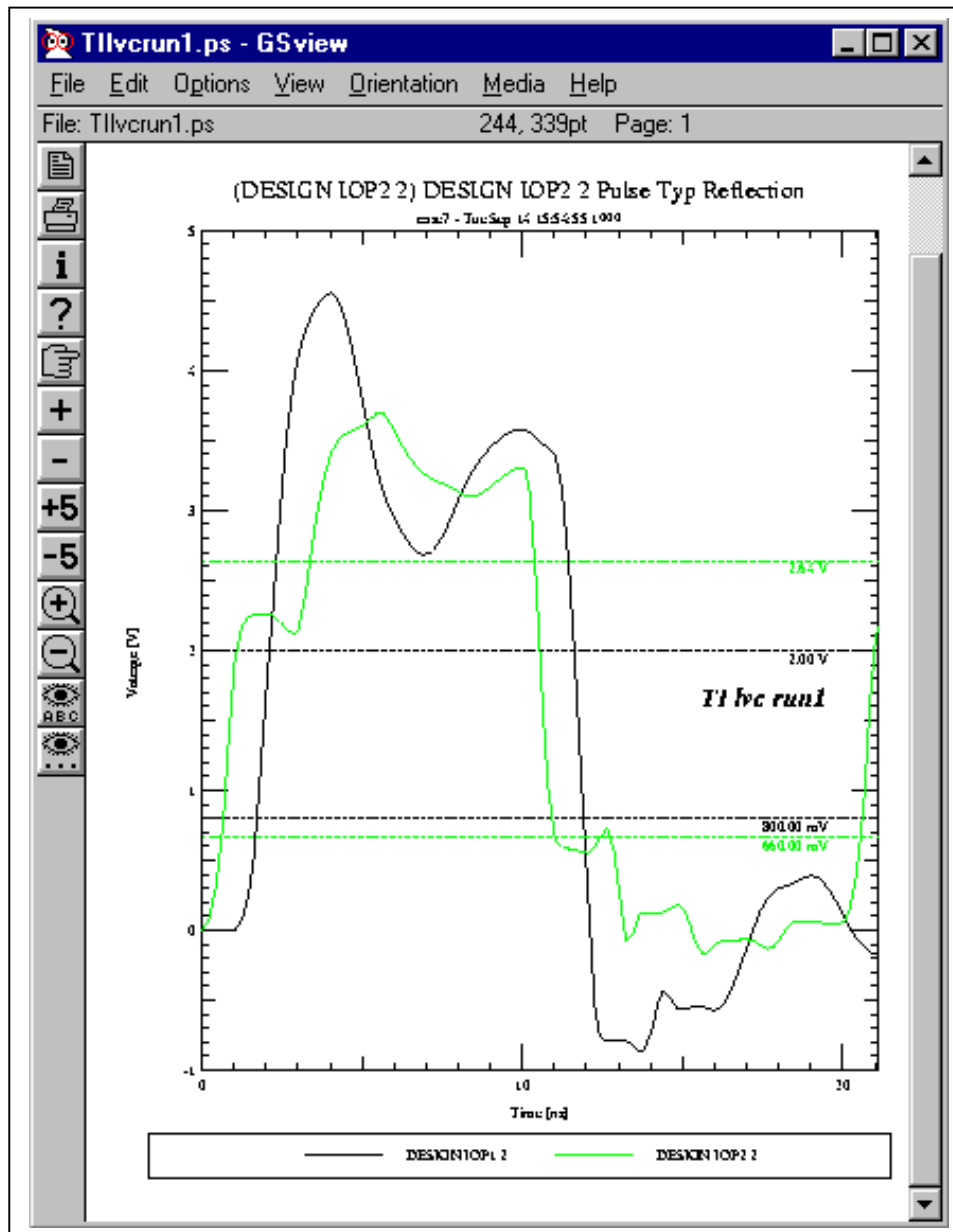
Phillips: Driver = 74LVC245\_OUT, Receiver = 74LVC245\_OUT  
Run3

Terminated



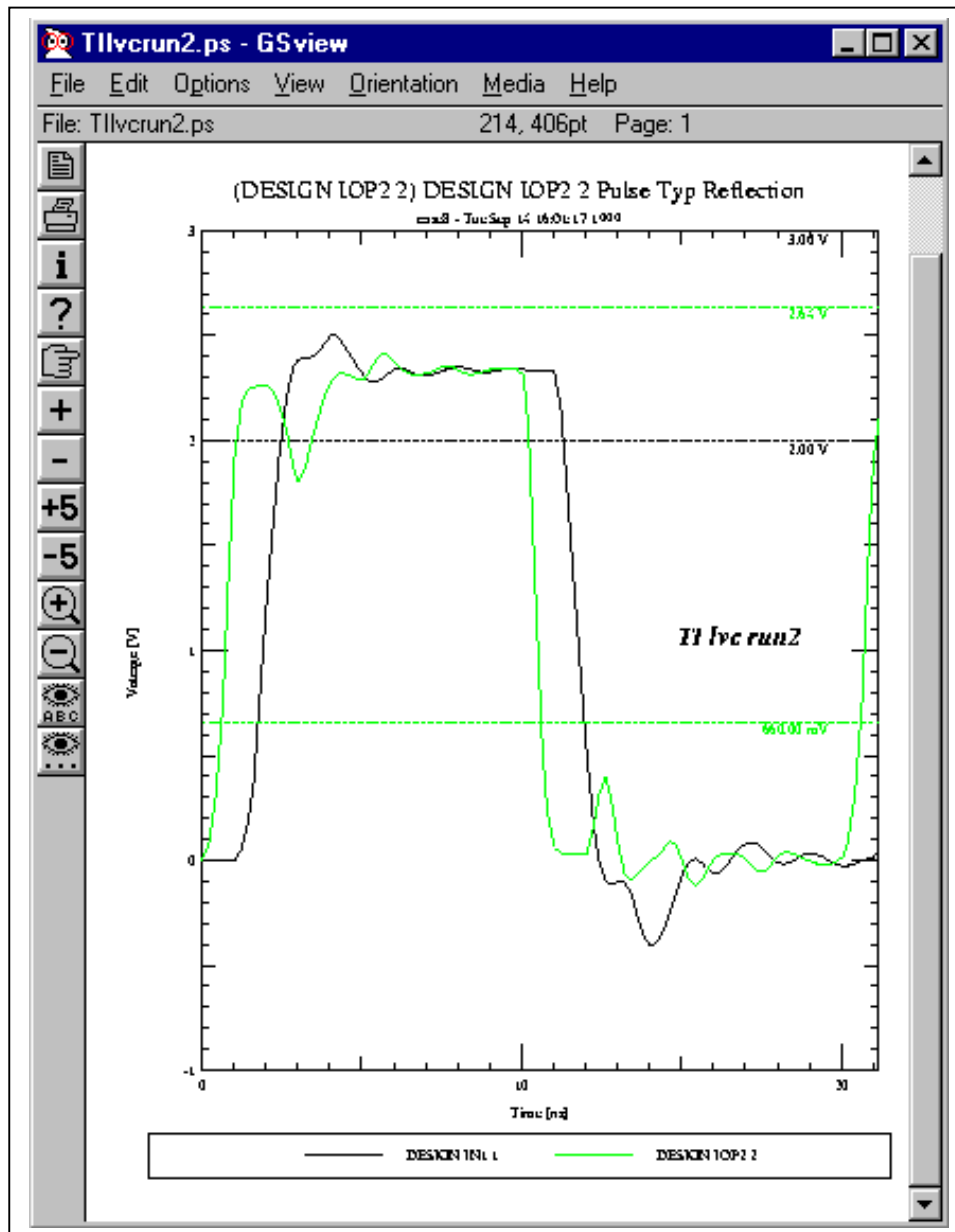
Phillips: Driver = 74LVC245\_OUT, Receiver = 74LVC245\_OUT  
Run3

Un-Terminated



TI: Driver = LVC16245A\_IO, Receiver = LVC16245A\_IO  
Run1

Terminated

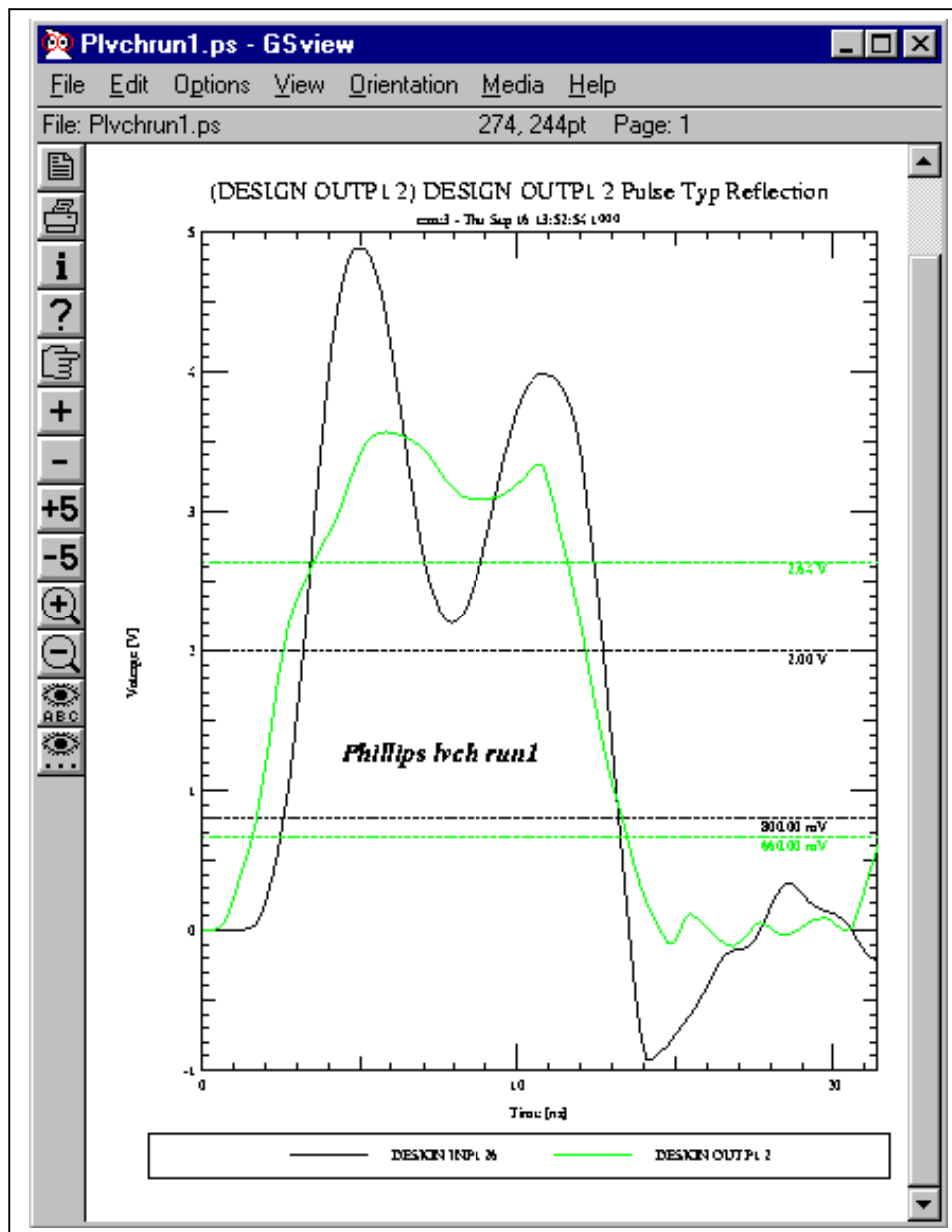


TI: Driver = LVC16245A\_IO, Receiver = LVC16245A\_IO  
Run2

## LVCH: Low Voltage CMOS Logic

Phillips

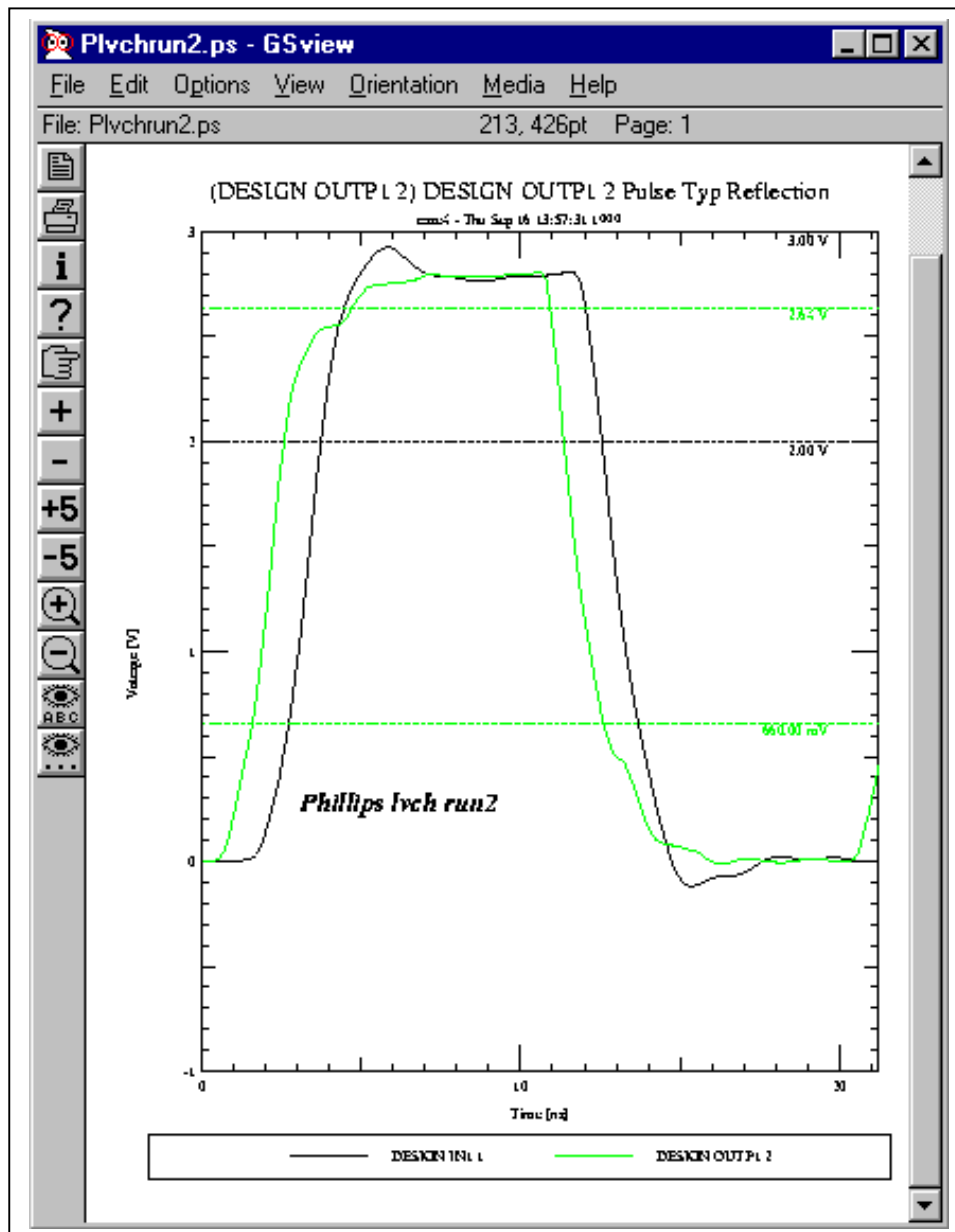
Un-Terminated



Phillips: Driver = 74LVCH16245\_OUT, Receiver = 74LVCH16245\_IN  
Run1



Terminated

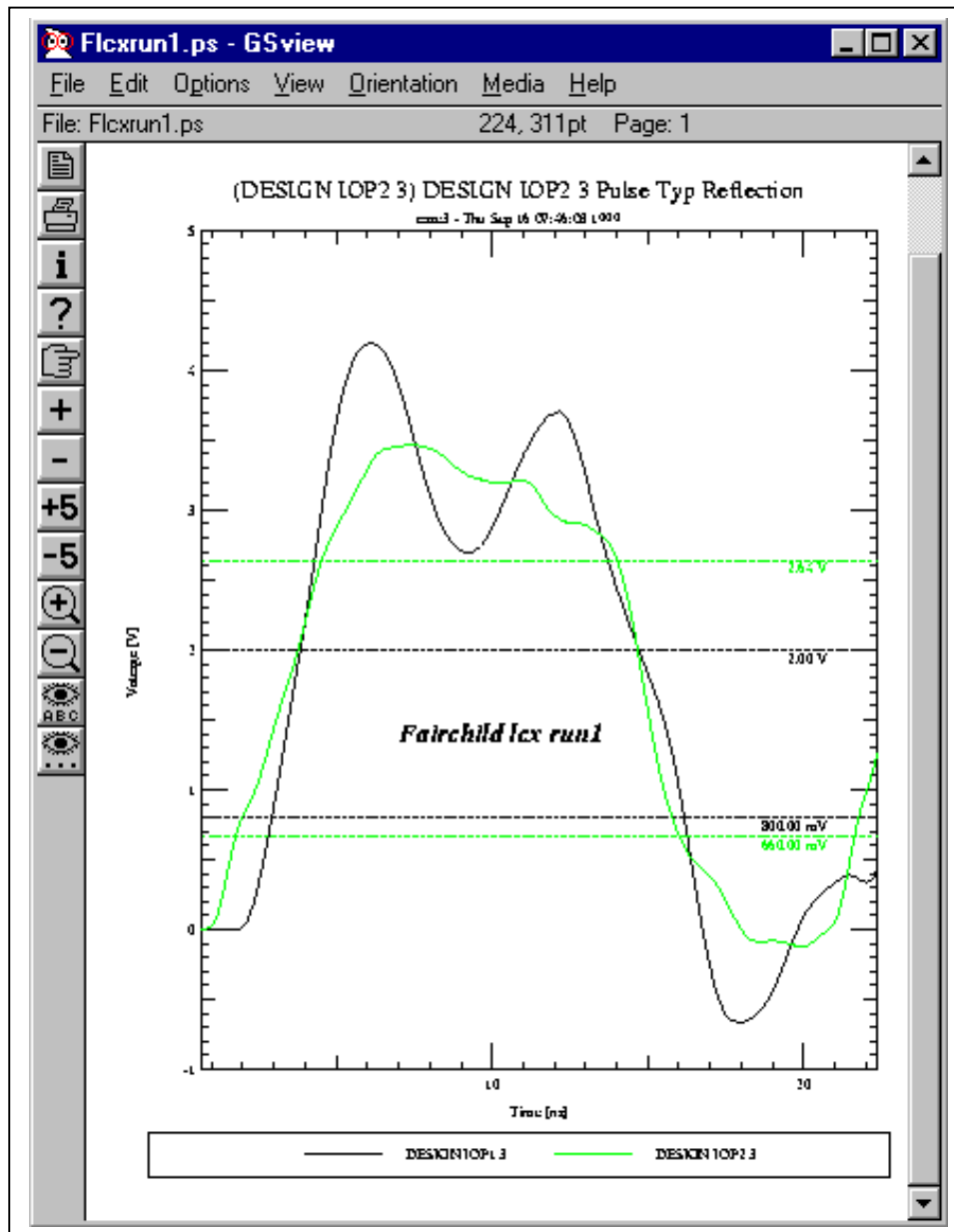


Phillips: Driver = 74LVCH16245\_OUT, Receiver = 74LVCH16245\_IN  
Run2

LCX

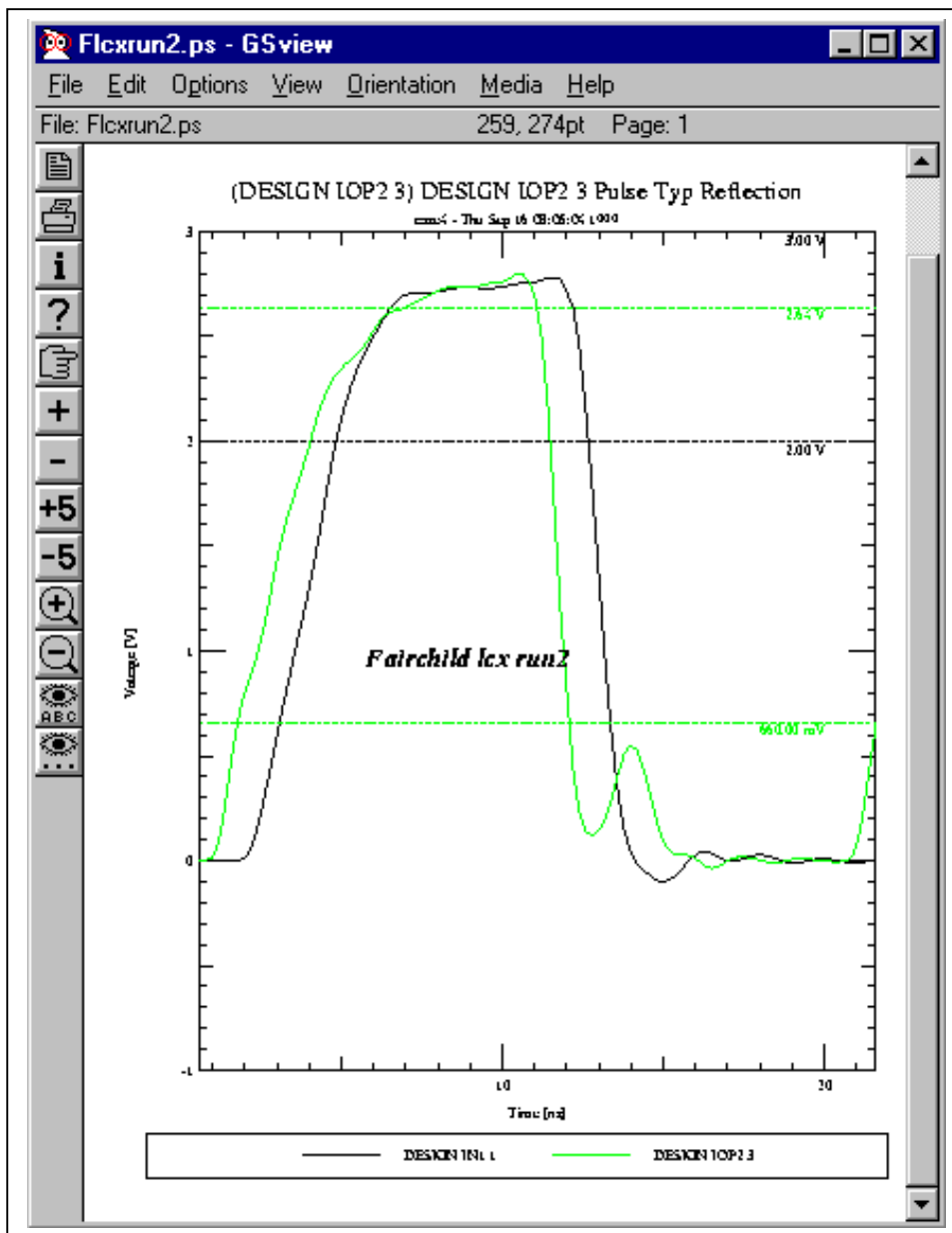
Fairchild

Un-Terminated



Fairchild: Driver = 74LCX245SC data\_io, Receiver = 74LCX245SC data\_io  
Run1

Terminated

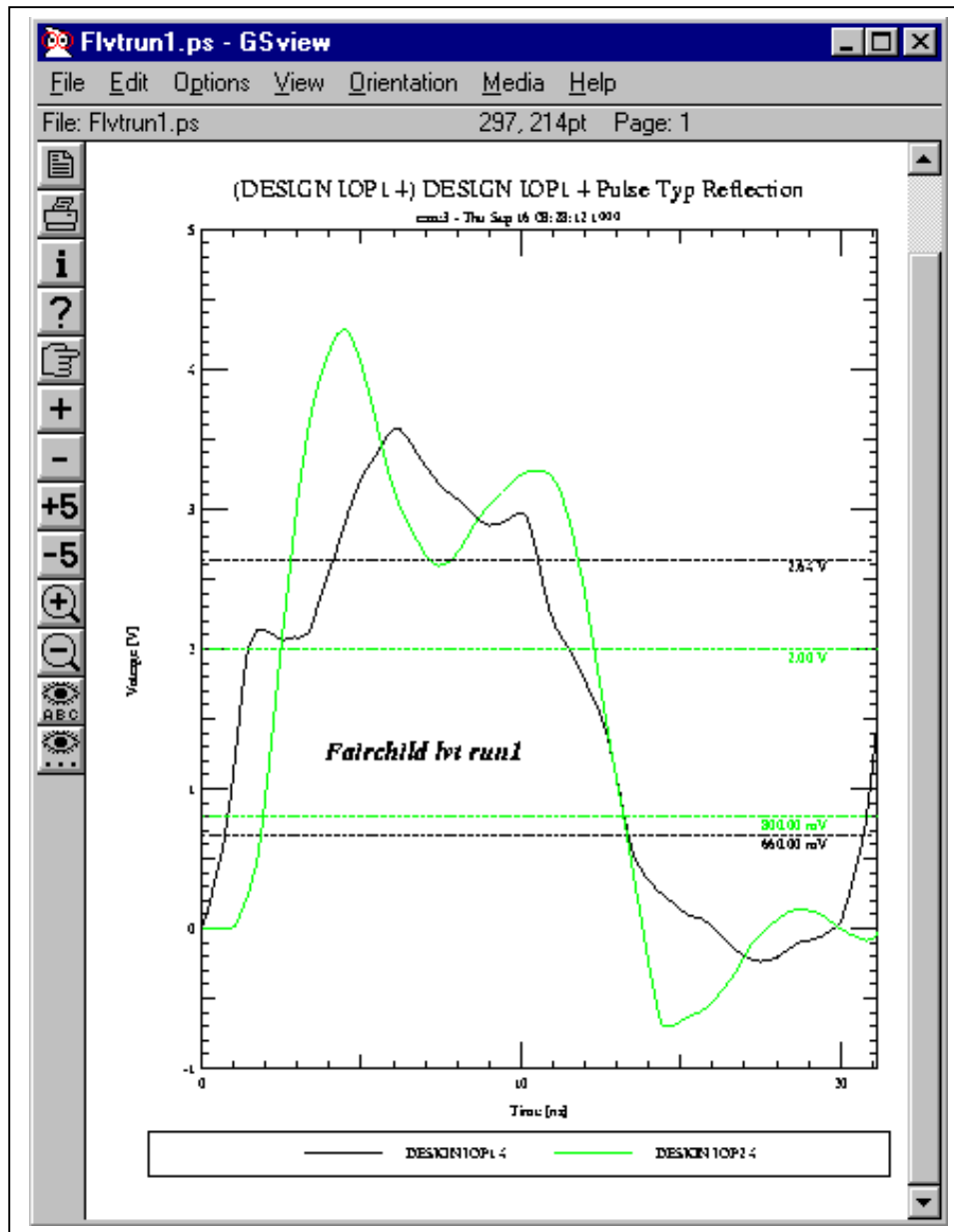


Fairchild: Driver = 74LCX245SC data\_io, Receiver = 74LCX245SC data\_io  
Run1

## LVT: Low Voltage BiCMOS Technology

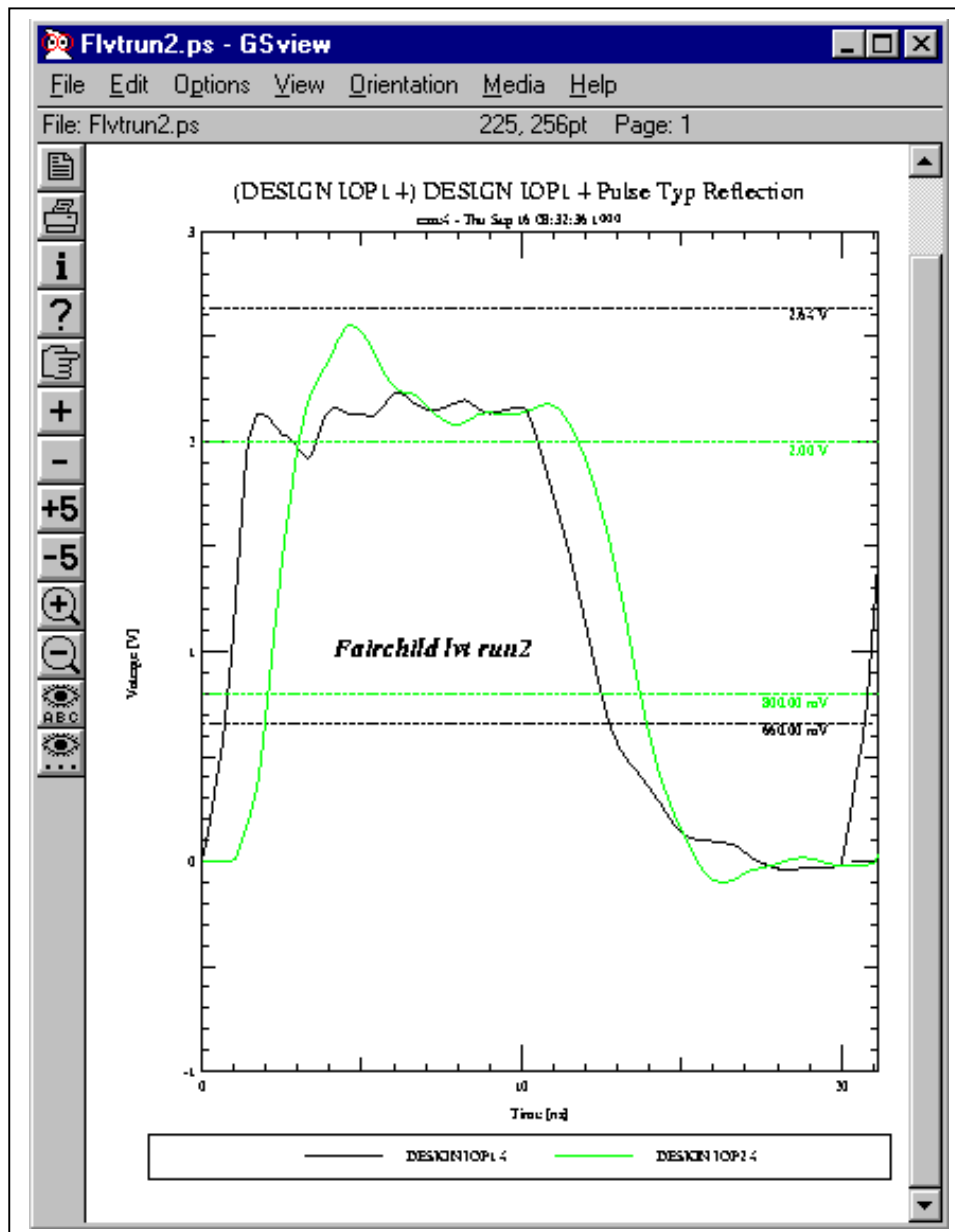
TI, Fairchild, Phillips

Un-Terminated



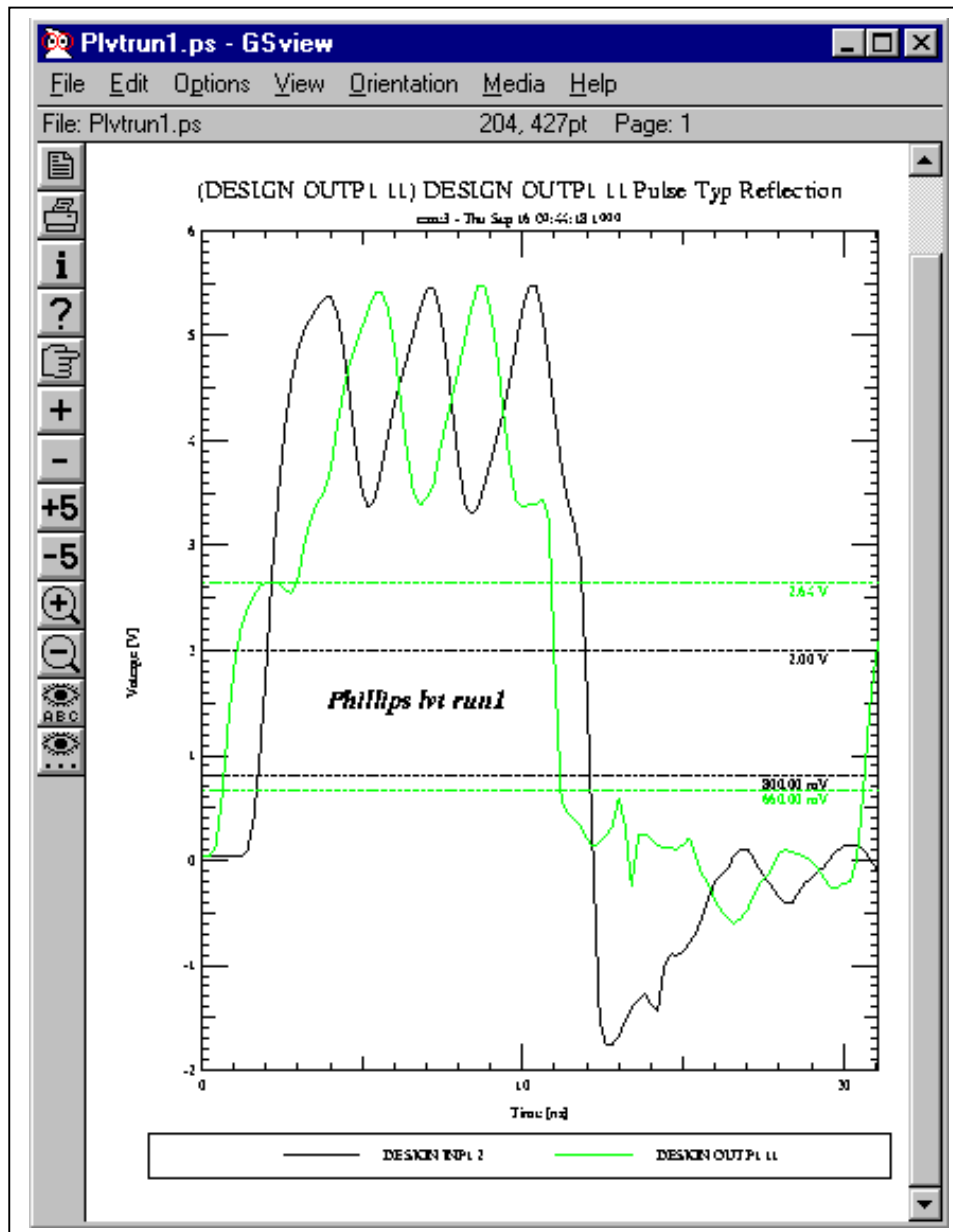
Fairchild: Driver = 74LVT245SC data\_io, Receiver = 74LVT245SC data\_io  
Run1

Terminated



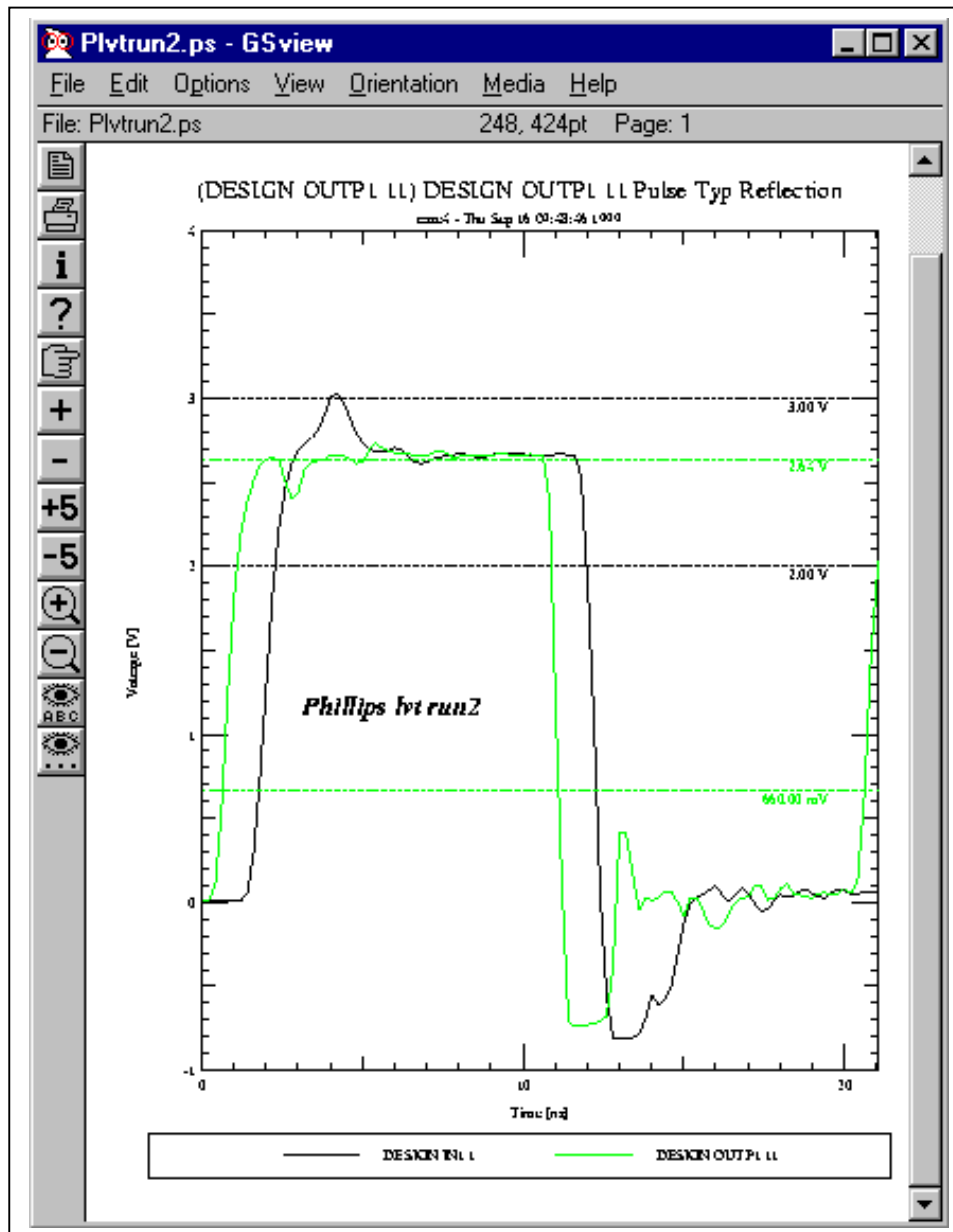
Fairchild: Driver = 74LVT245SC data\_io, Receiver = 74LVT245SC data\_io  
Run2

## Un-Terminated



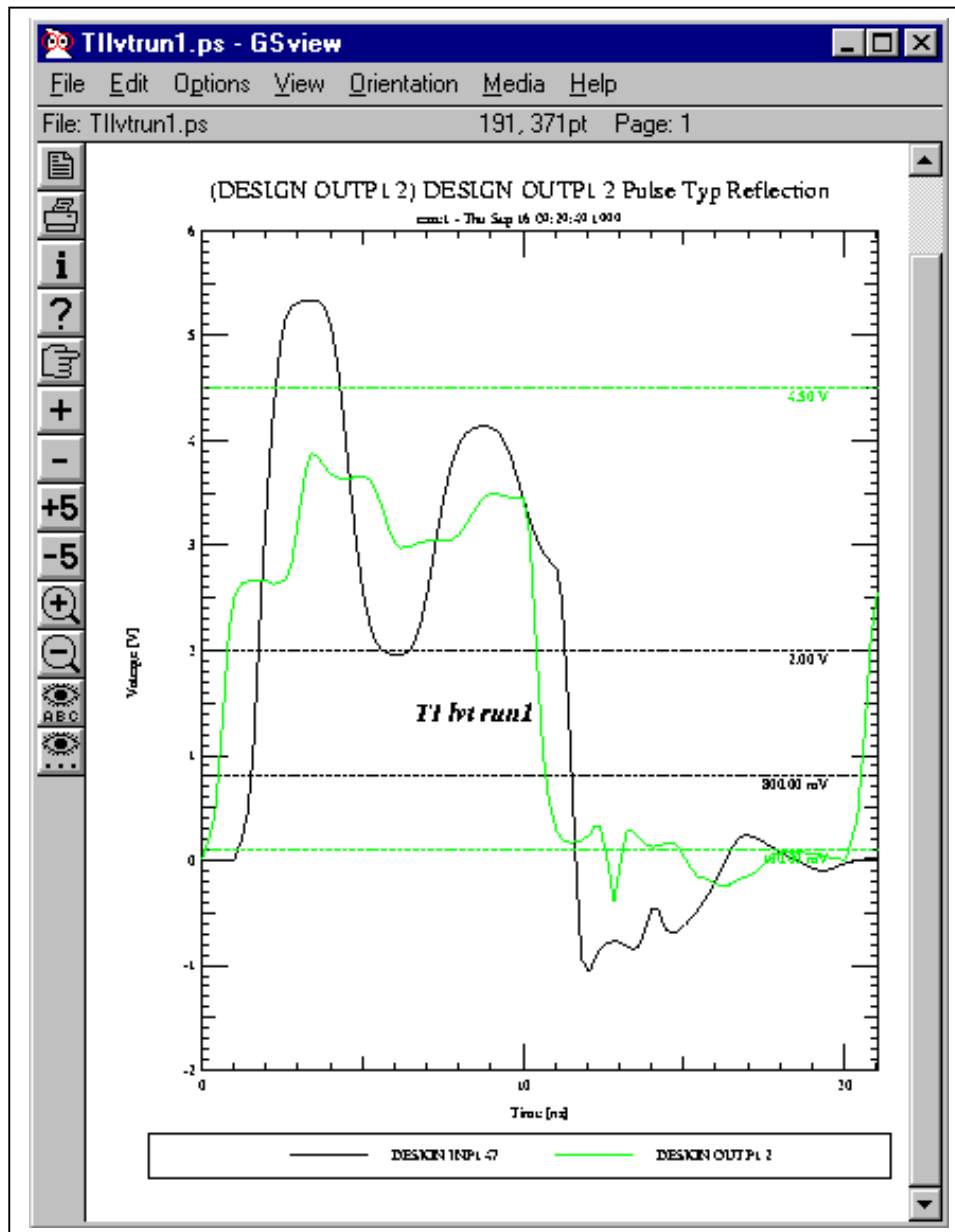
Phillips: Driver = 74LVT245\_OUT, Receiver = 74LVT245\_IN  
Run1

Terminated



Phillips: Driver = 74LVT245\_OUT, Receiver = 74LVT245\_IN  
Run2

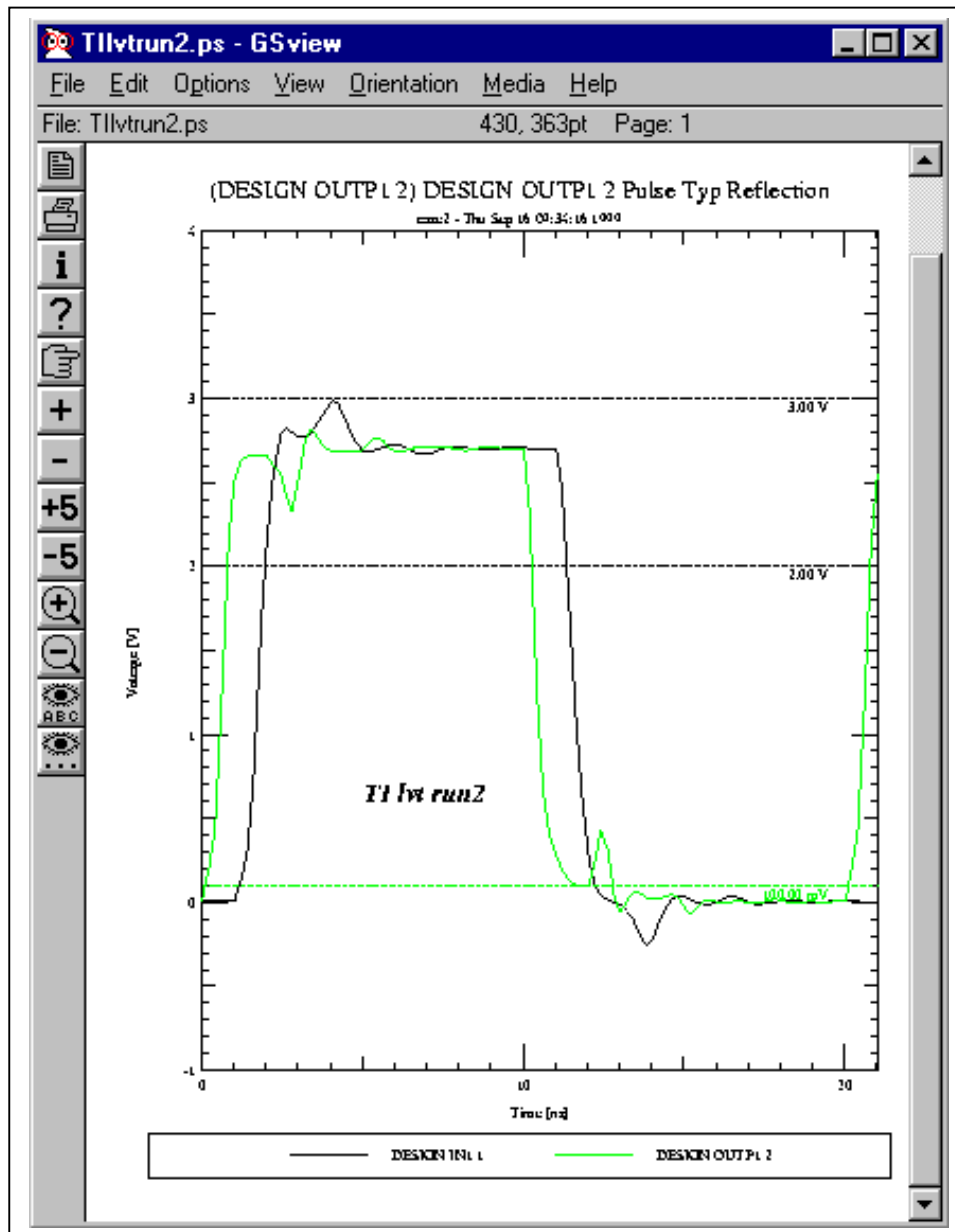
Un-Terminated



TI: Driver = LVT16244A\_OUT, Receiver = LVT16244A\_IN  
Run1



Terminated

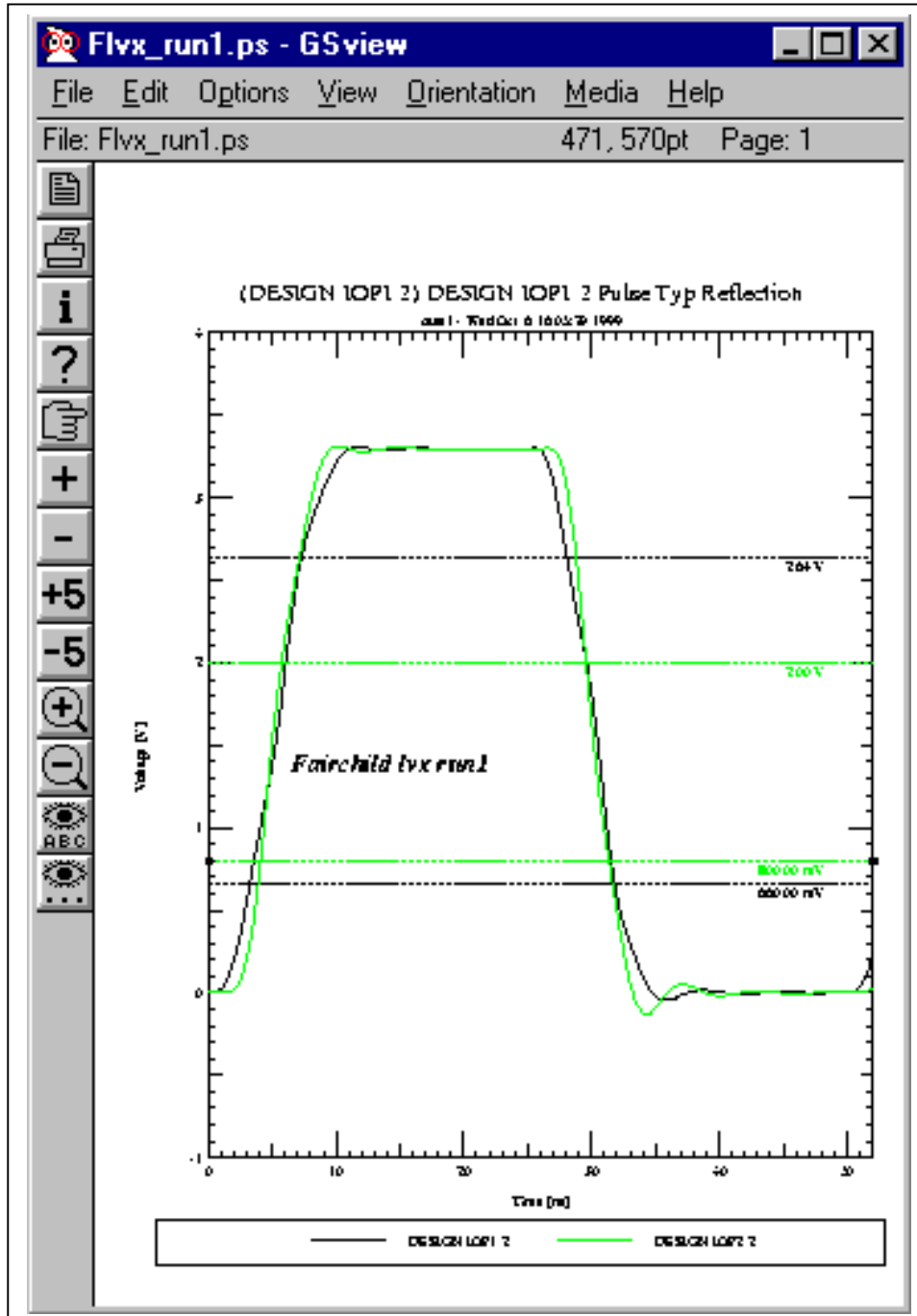


TI: Driver = LVT16244A\_OUT, Receiver = LVT16244A\_IN  
Run2

**LVX:**

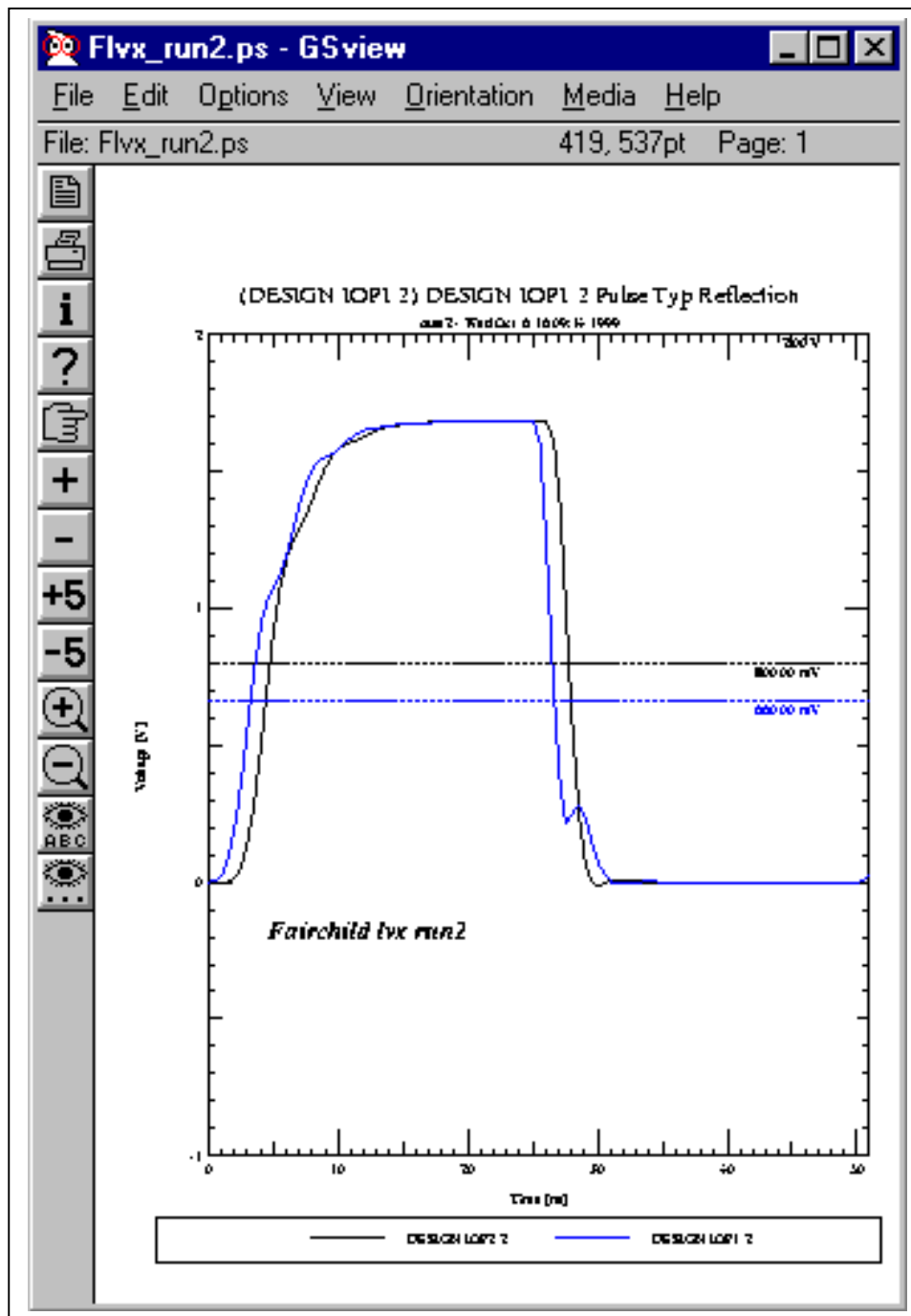
Fairchild

Un-Terminated



Fairchild: Driver = 74LVX245SC data\_io, Receiver = 74LVX245SC data\_io  
Run1

Terminated

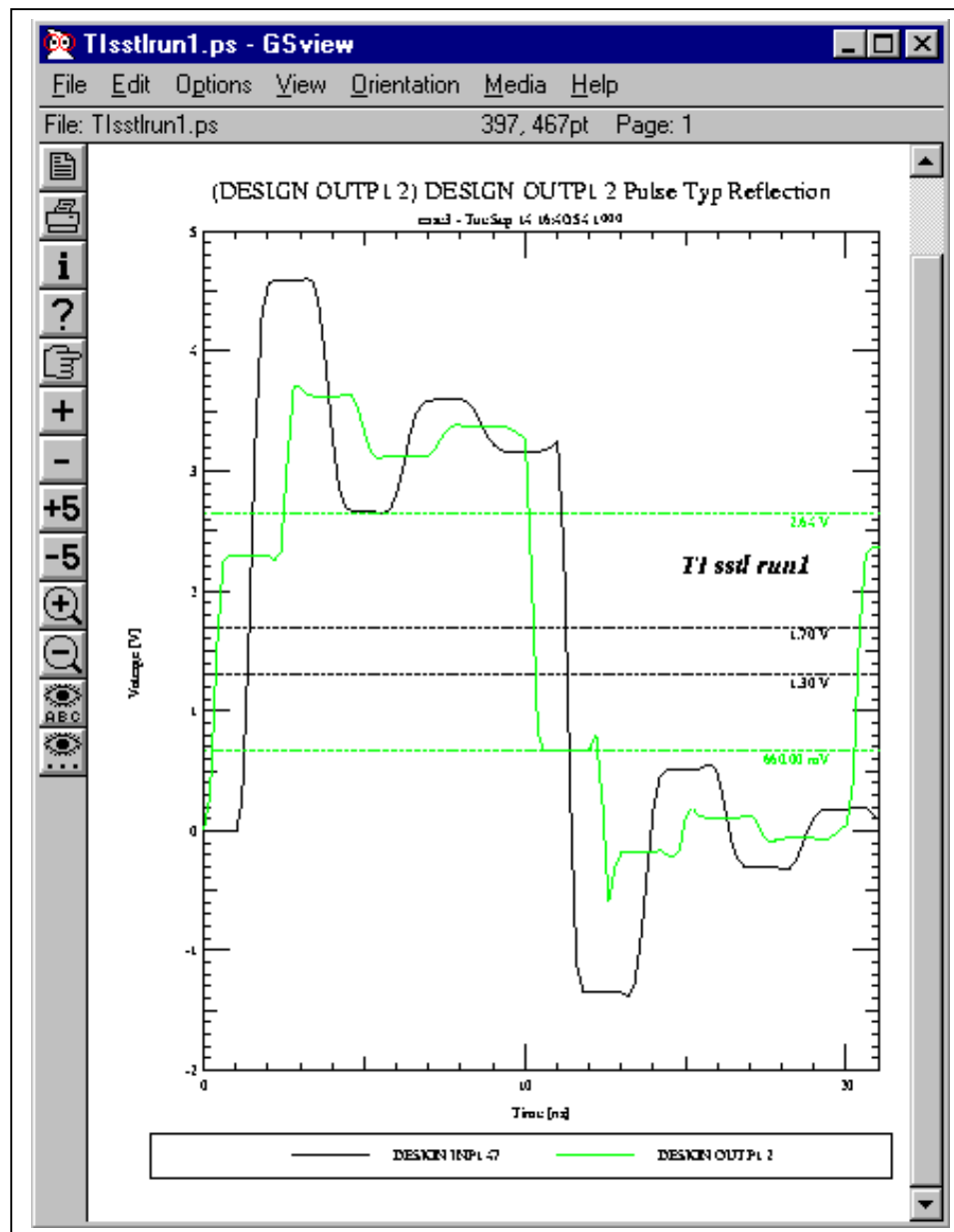


Fairchild: Driver = 74LVX245SC data\_io, Receiver = 74LVX245SC data\_io  
Run2

## SSTL: Stub Series Terminated Logic

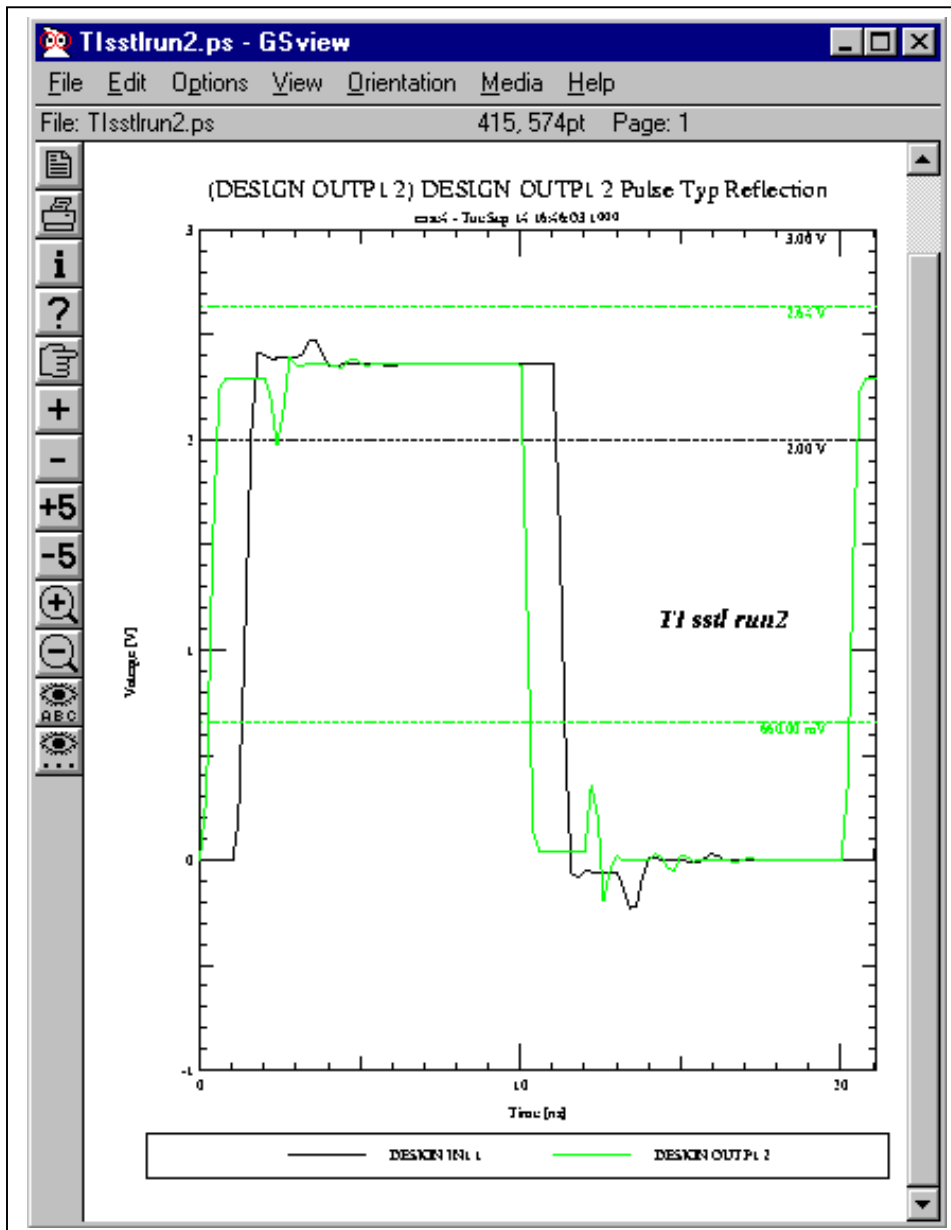
TI

Un-Terminated



TI: Driver = SSTL16837\_OUT, Receiver = SSTL16837\_IN  
Run1

Terminated



TI: Driver = SSTL16837\_OUT, Receiver = SSTL16837\_IN  
Run1

## **2.5 Volt Logic**

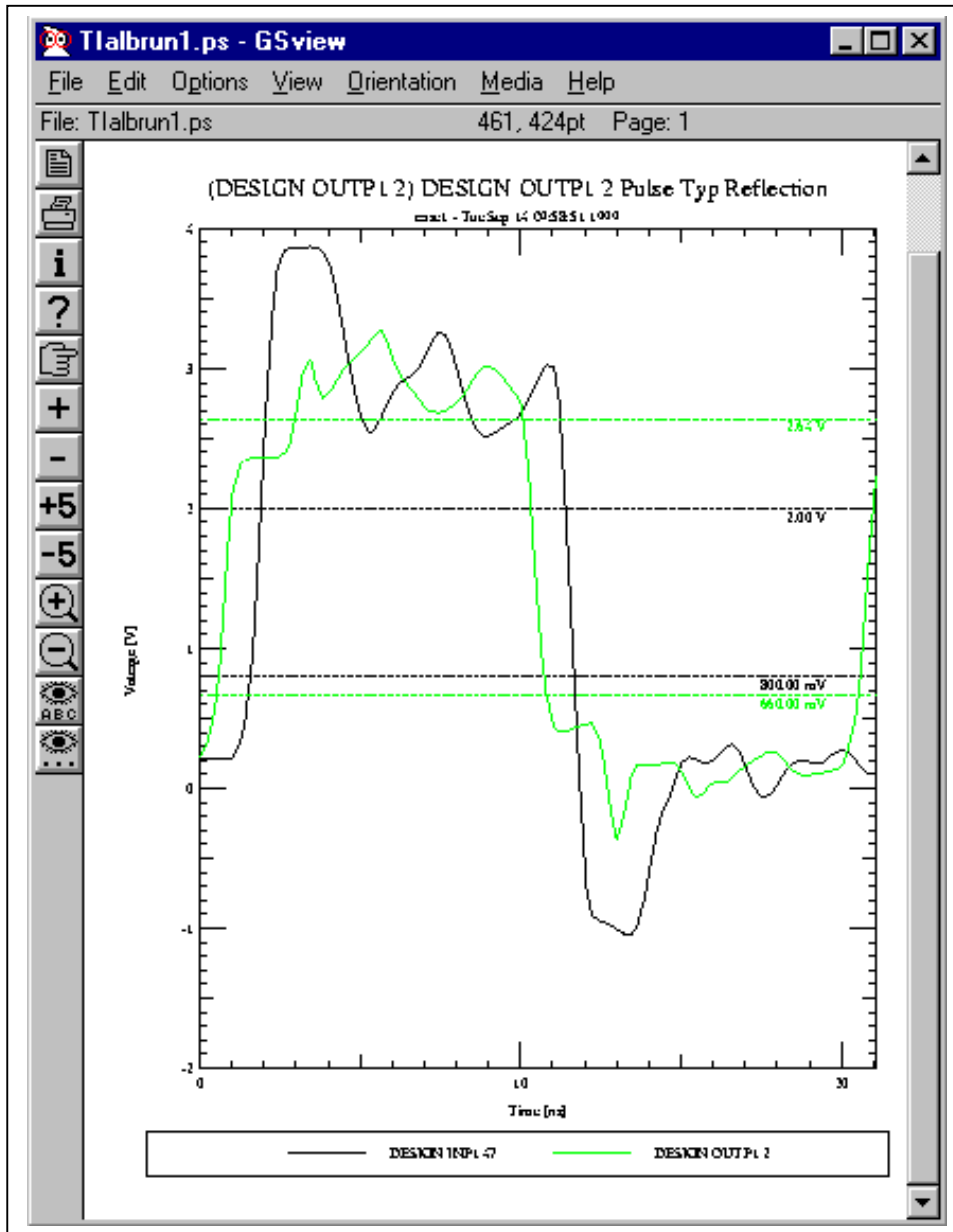
CMOS: ALVC, ALVT, LVC, VCX

BiCMOS: ALB, F/FAST

## ALB: Advanced Low Voltage BiCMOS Technology

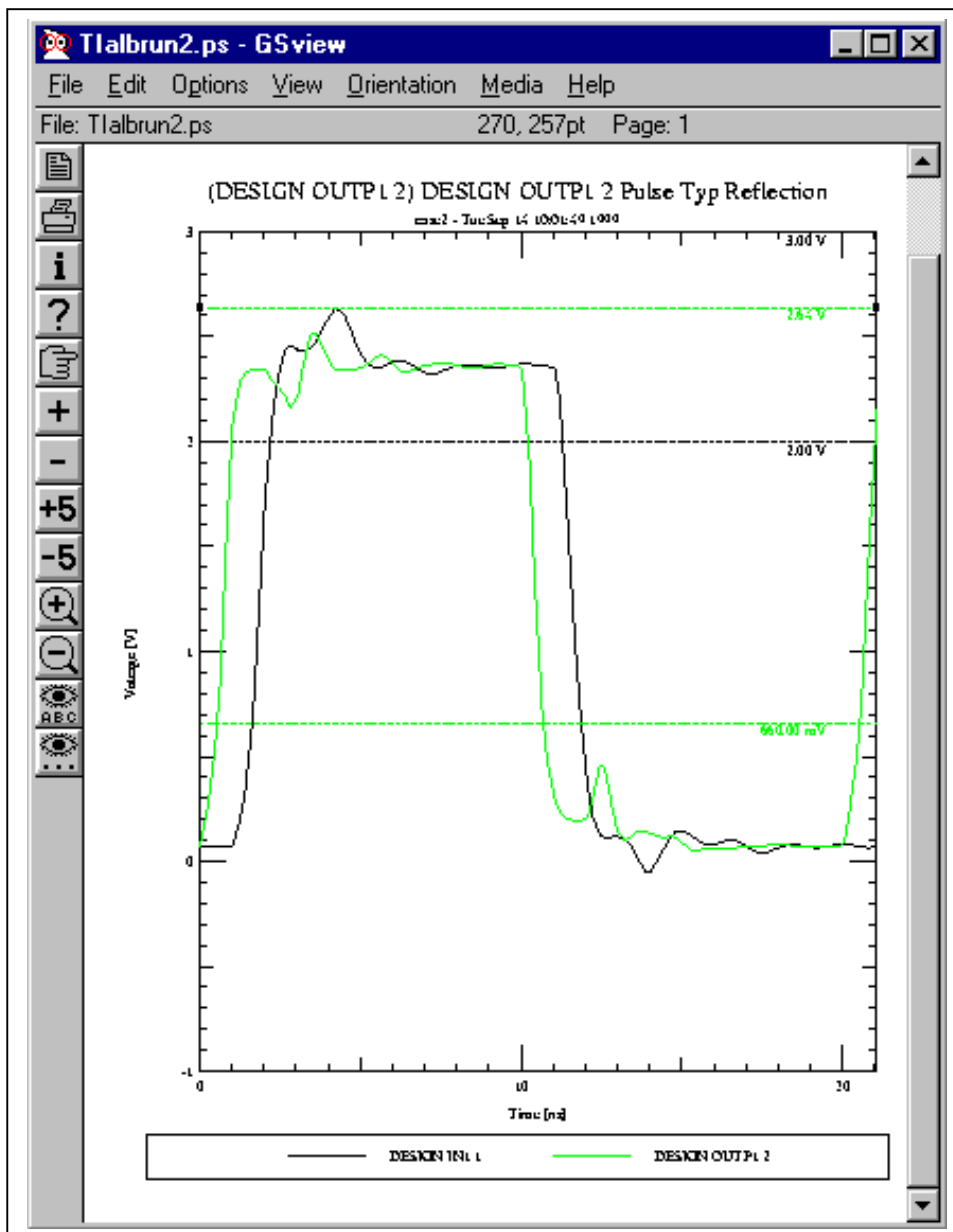
TI

Un-Terminated



TI: Driver = ALB16244\_OUT, Receiver = ALB16244\_IN  
Run1

Terminated



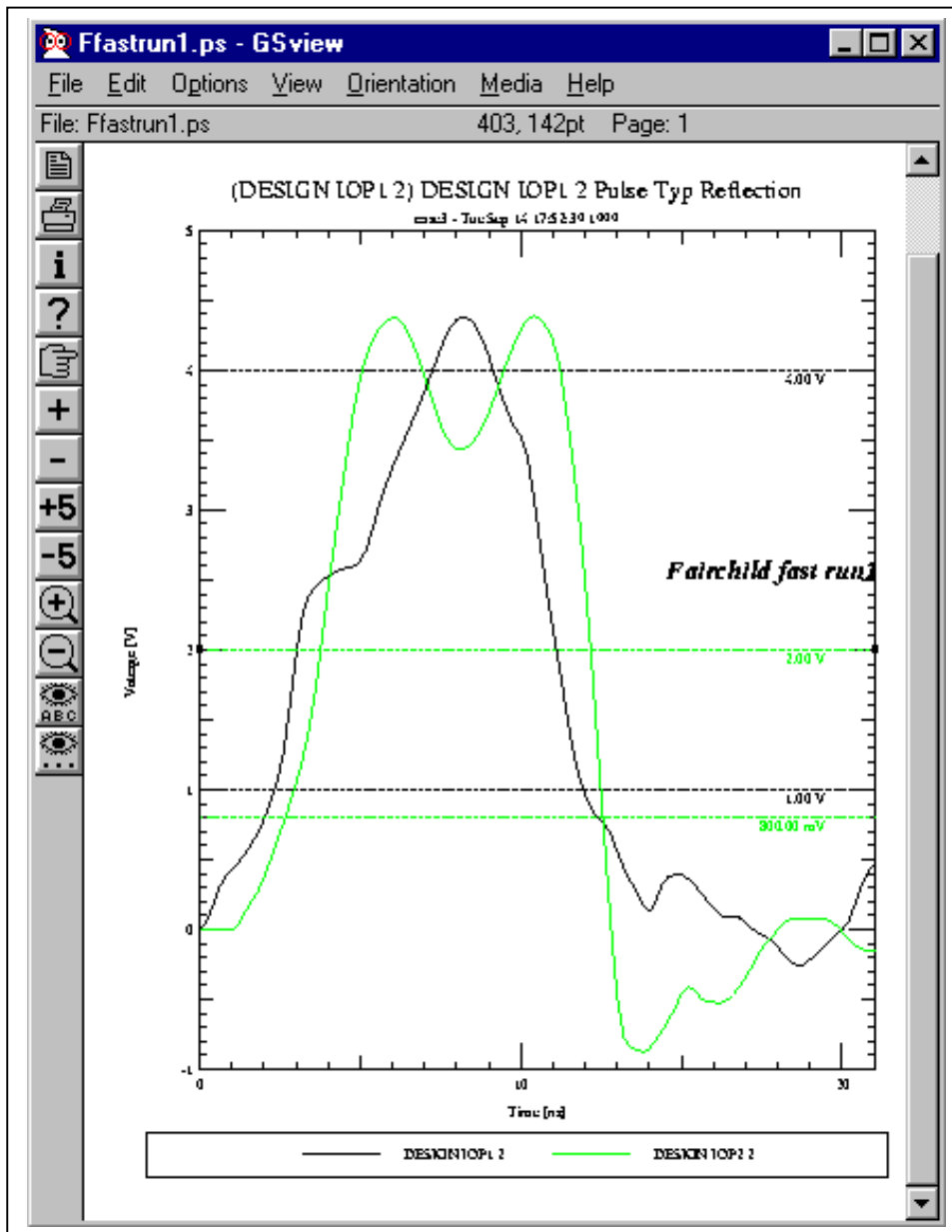
TI: Driver = ALB16244\_OUT, Receiver = ALB16244\_IN  
Run2



## F/FAST: F Logic

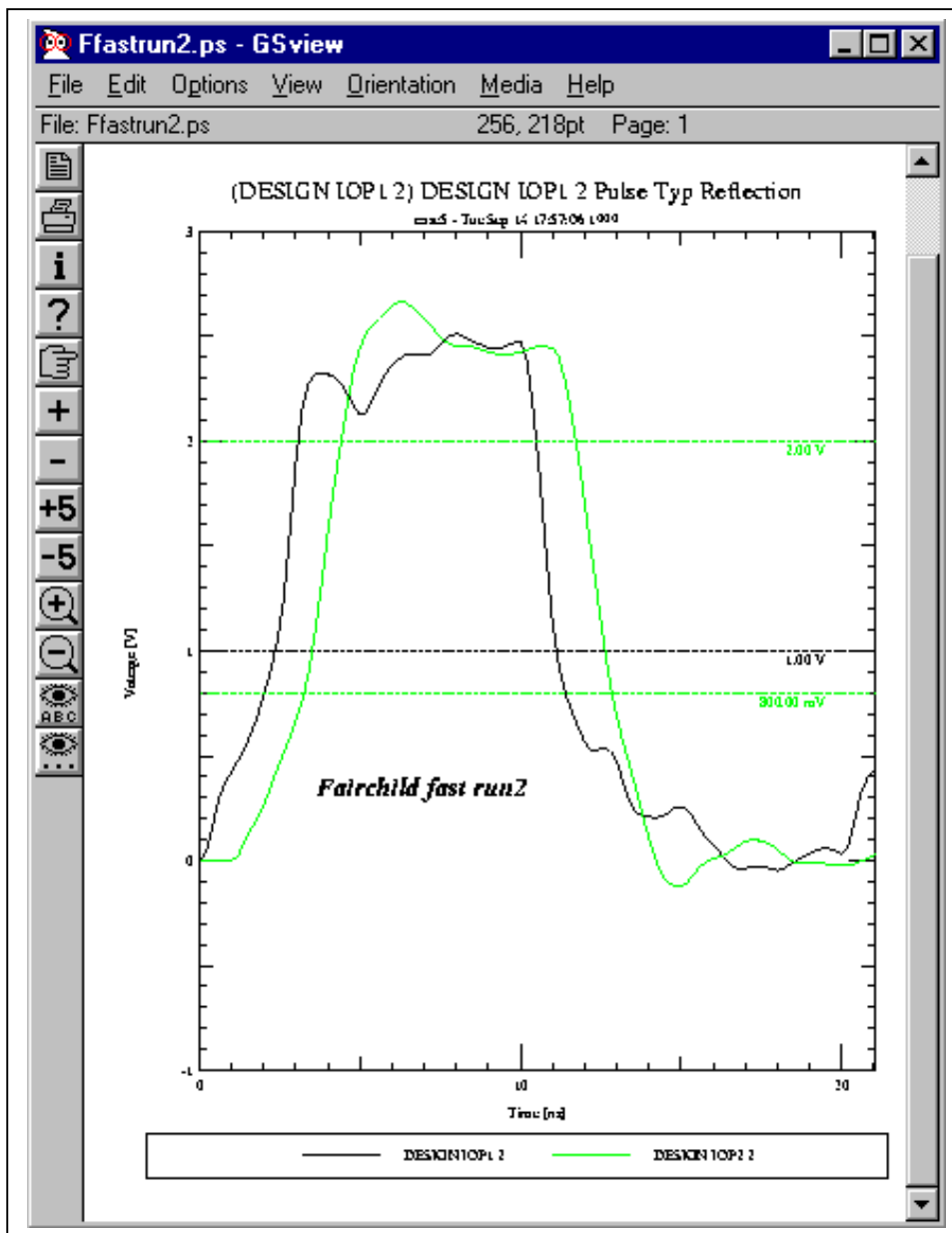
Fairchild, TI

Un-Terminated



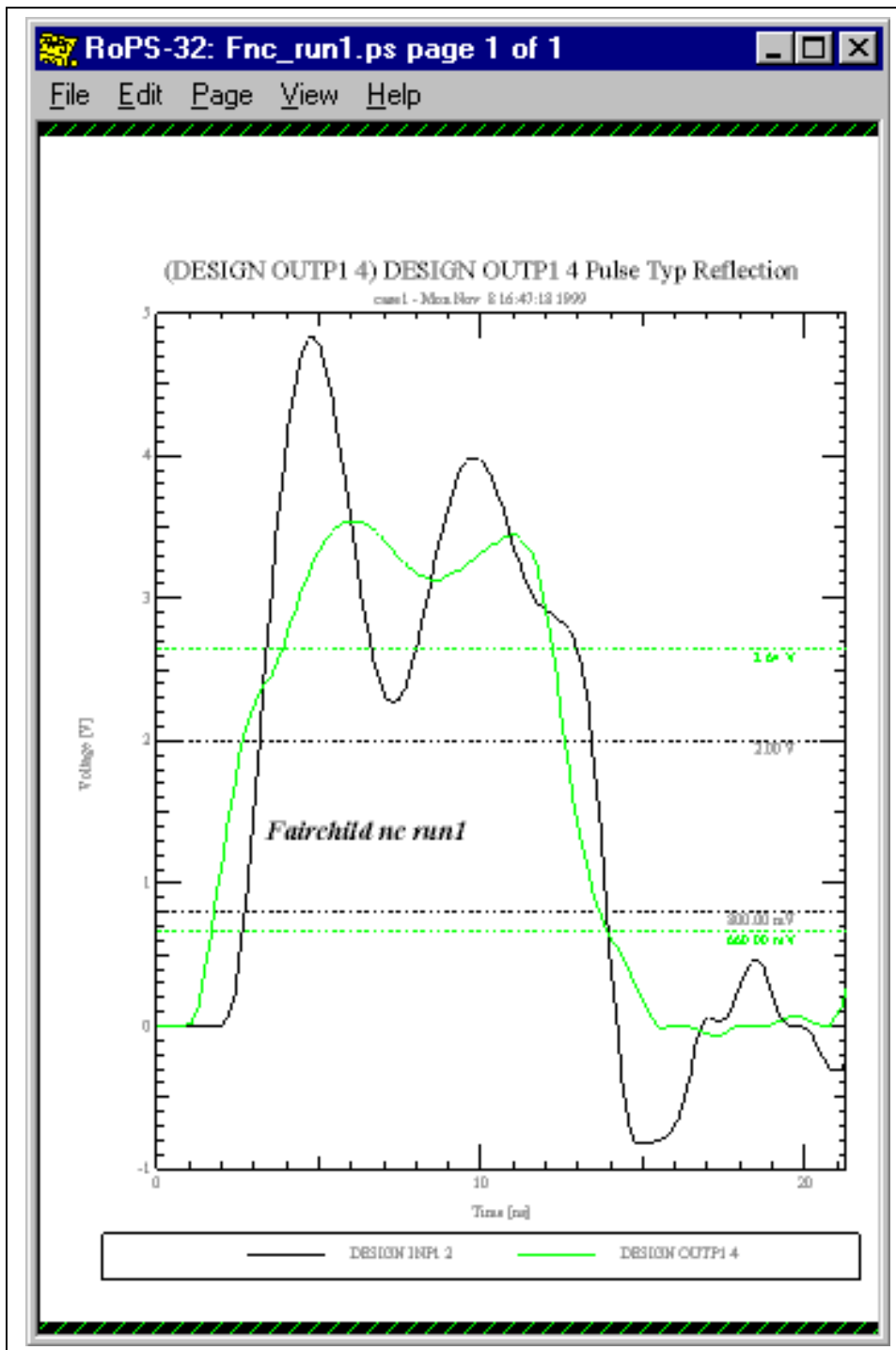
Fairchild: Driver = 74F245SC data\_io, Receiver = 74F245SC data\_io  
Run1

Terminated



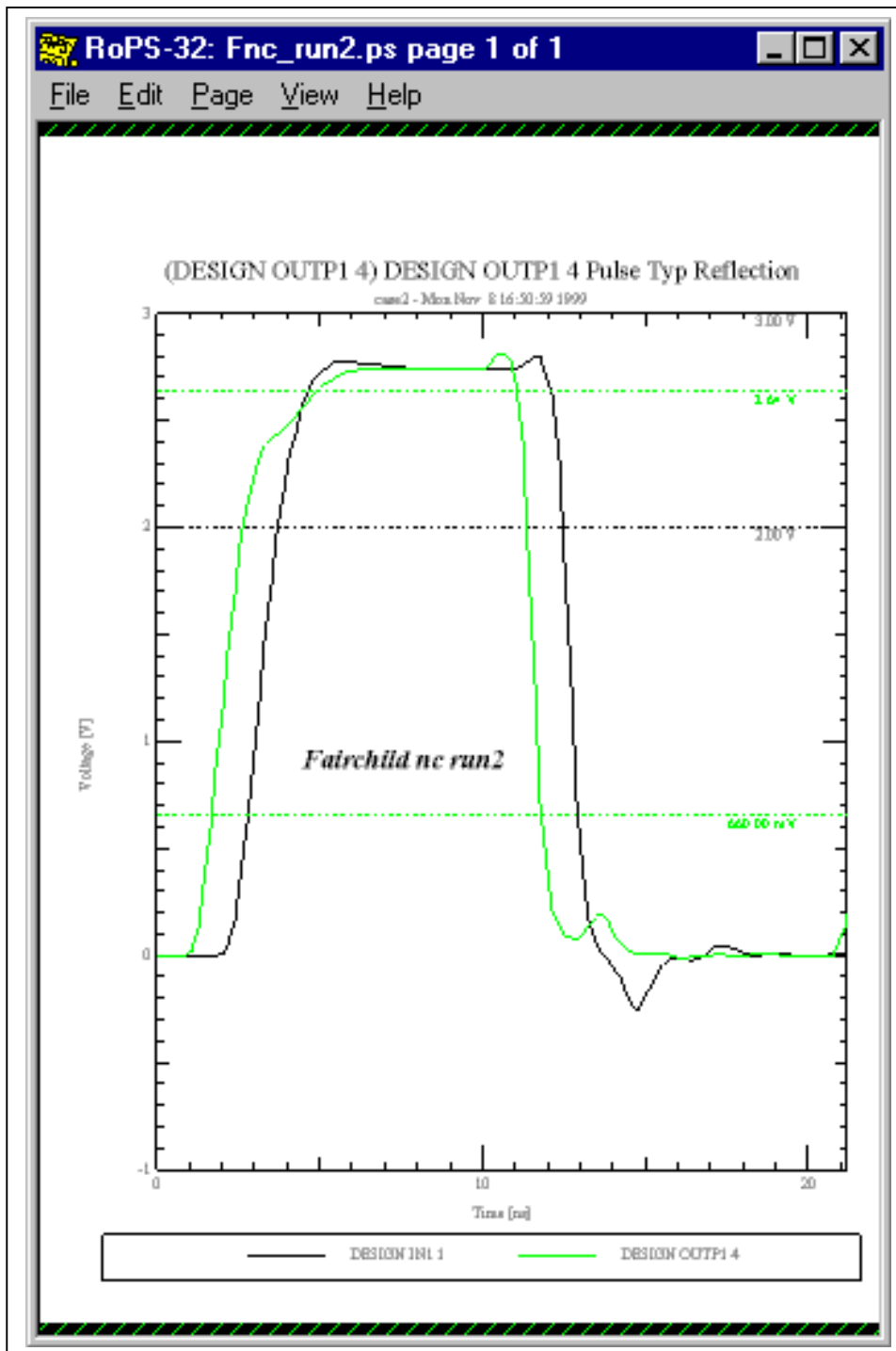
Fairchild: Driver = 74F245SC data\_io, Receiver = 74F245SC data\_io  
Run1

NC:  
Fairchild  
Terminated



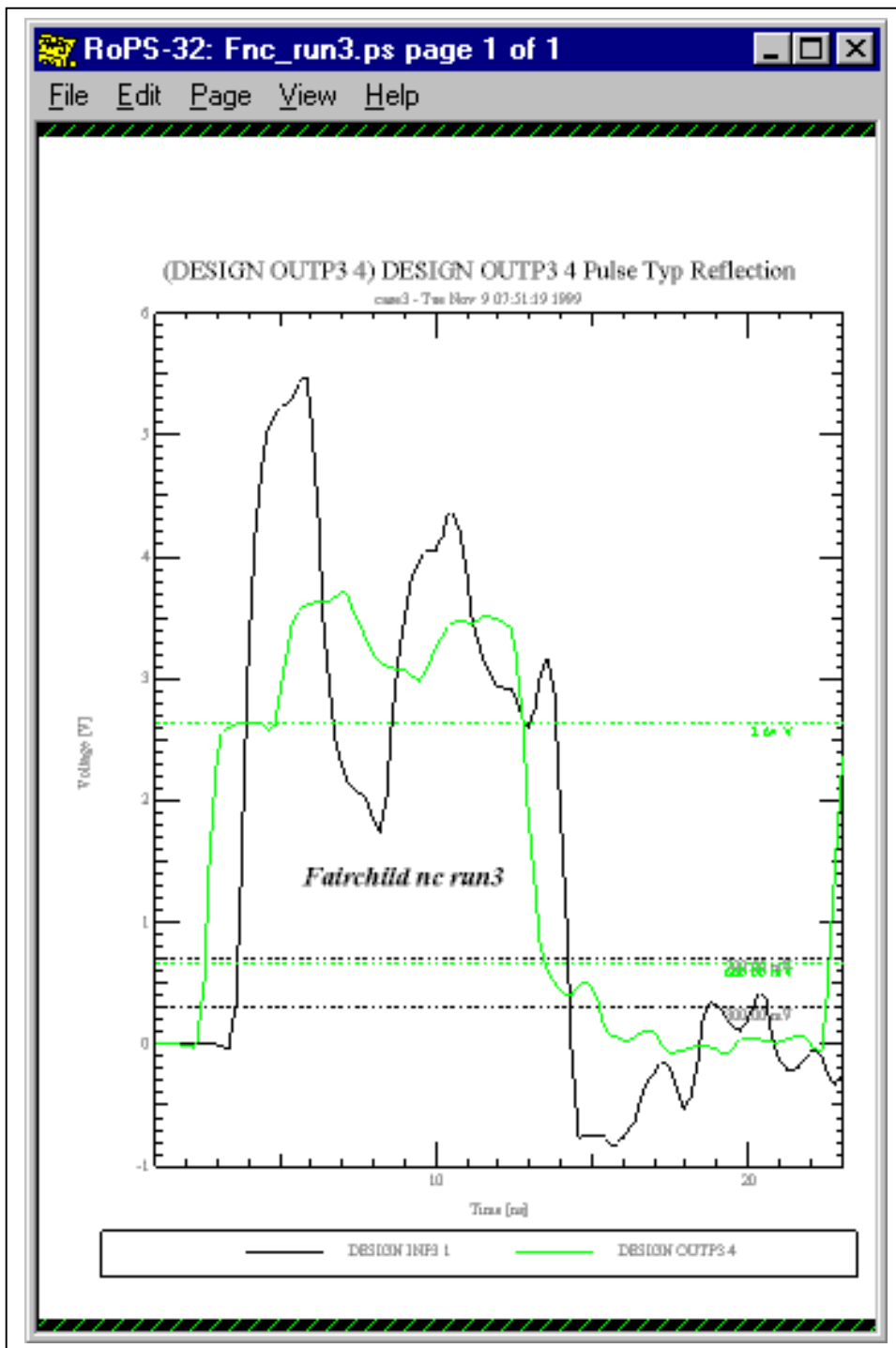
Fairchild NC: Driver = 74NC7SZ125\_out, Receiver = 74NC7SZ125\_in  
Run1

Terminated



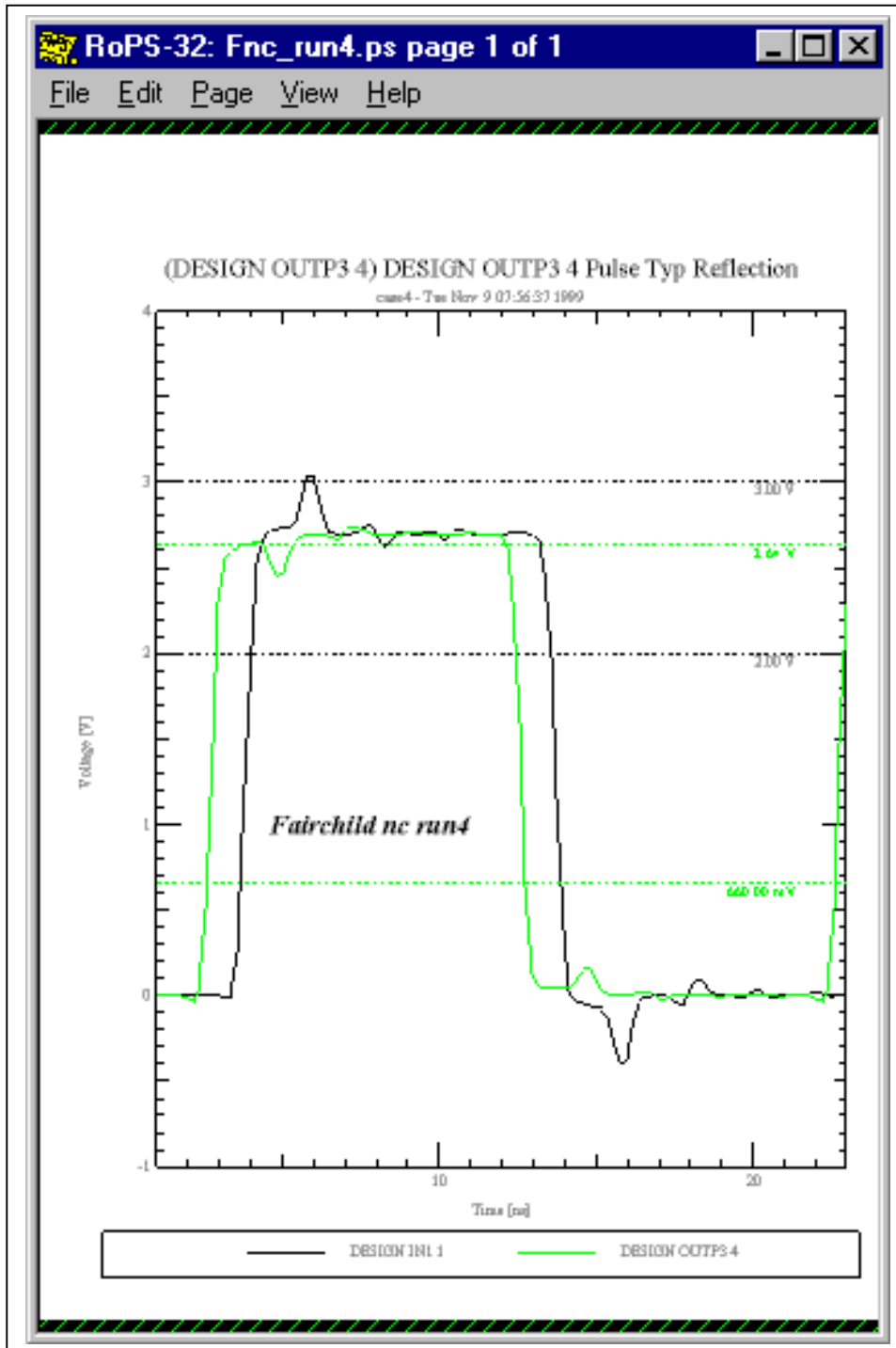
Fairchild NC: Driver = 74NC7SZ125\_out, Receiver = 74NC7SZ125\_in  
Run2

Unterminated



Fairchild NC: Driver = 74NC7WZ04\_data\_out, Receiver = 74NC7WZ04\_data\_in  
Run3

Terminated

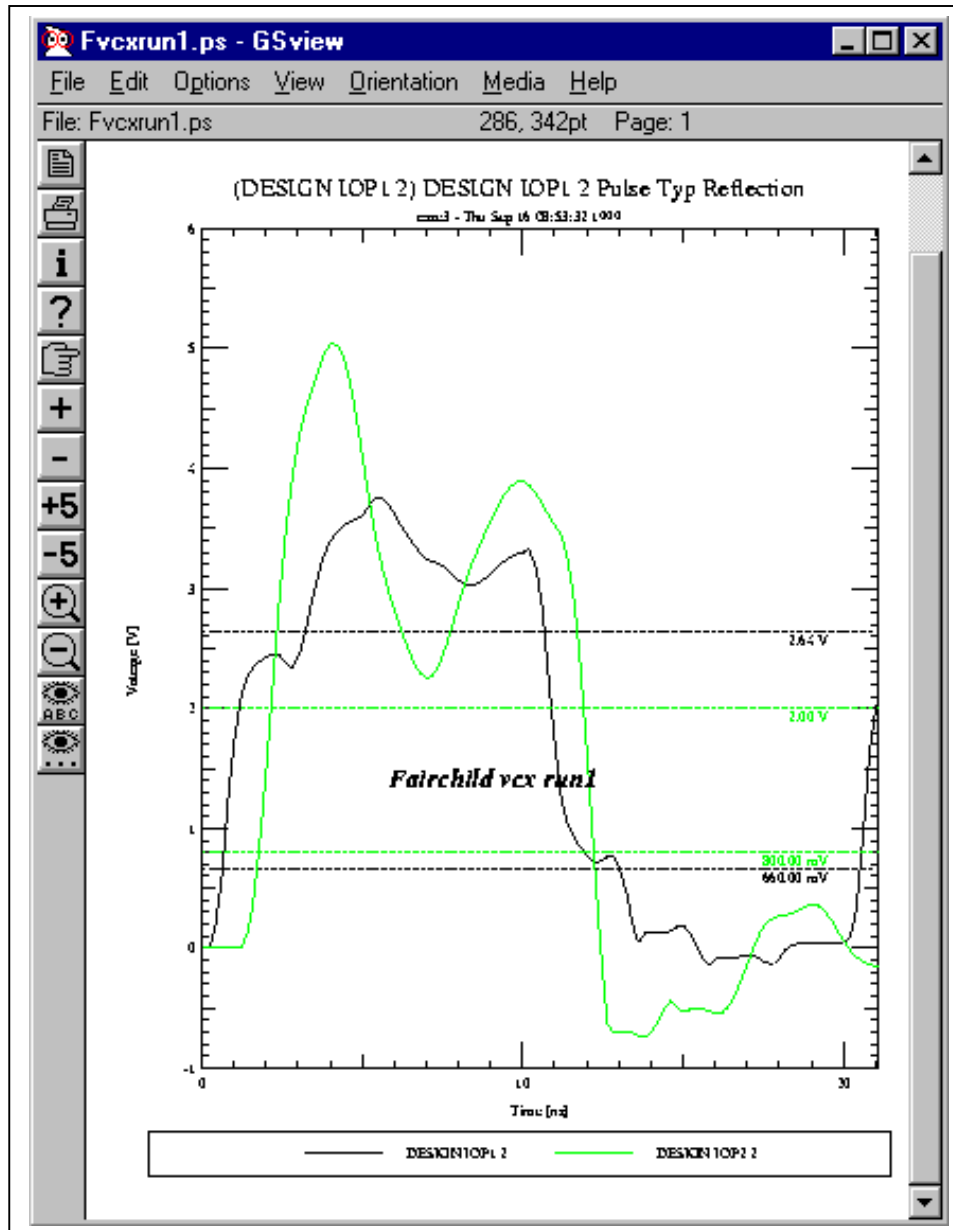


Fairchild NC: Driver = 74NC7WZ04\_data\_out, Receiver = 74NC7WZ04\_data\_in  
Run4

VCX

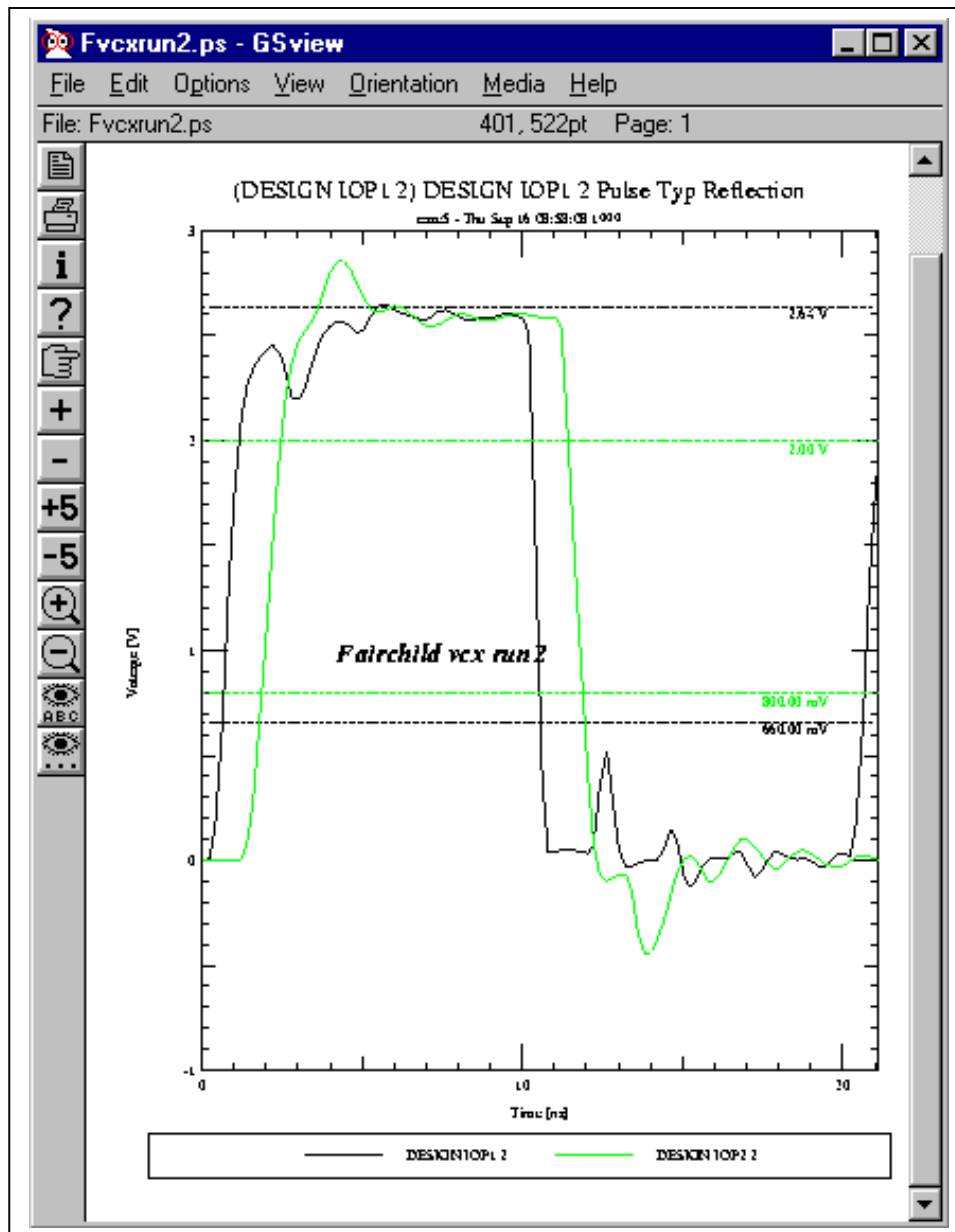
Fairchild

Un-Terminated



Fairchild: Driver = 74VCX16245MTD data\_io, Receiver = 74VCX16245MTD data\_io  
Run1

Terminated



Fairchild: Driver = 74VCX16245MTD data\_io, Receiver = 74VCX16245MTD data\_io  
Run2





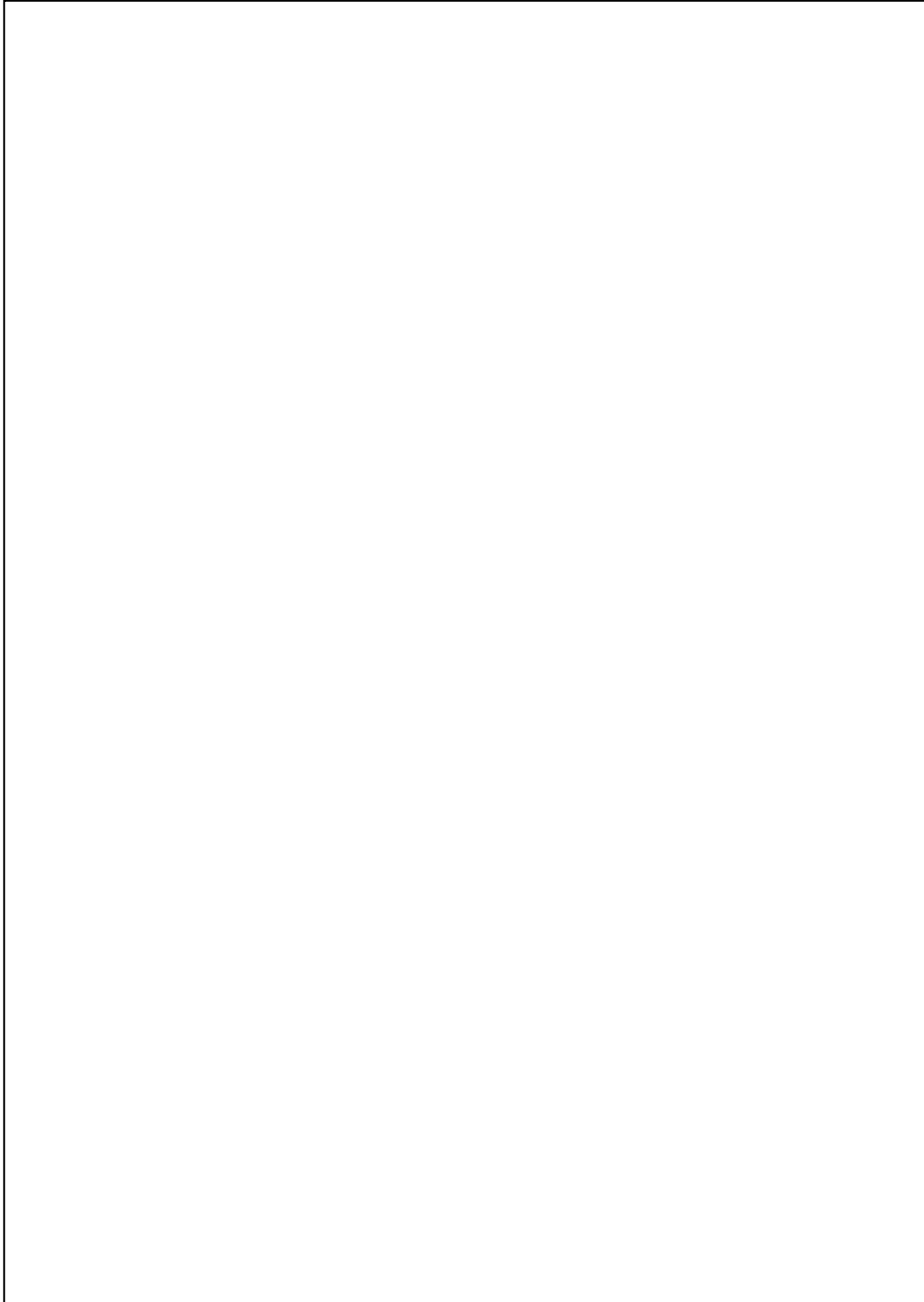
## **2.5/2.1 Volt Logic (Backplane Technology)**

BCT, BTL/ FB+, CBT, CBTLV, GTL/GTLP+

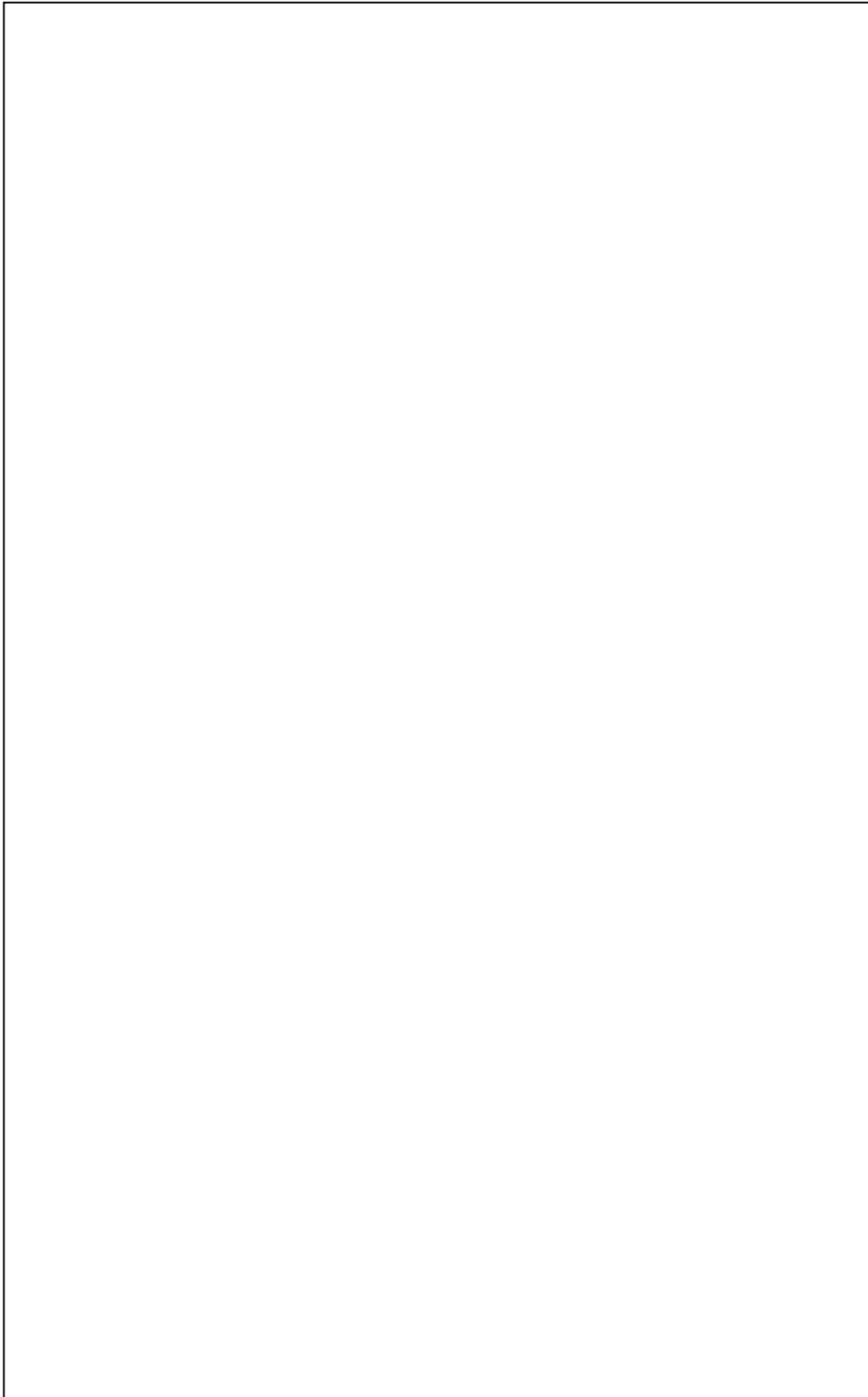
**\*BCT**

BiCMOS Bus Interface Technology  
TI

Un-Terminated



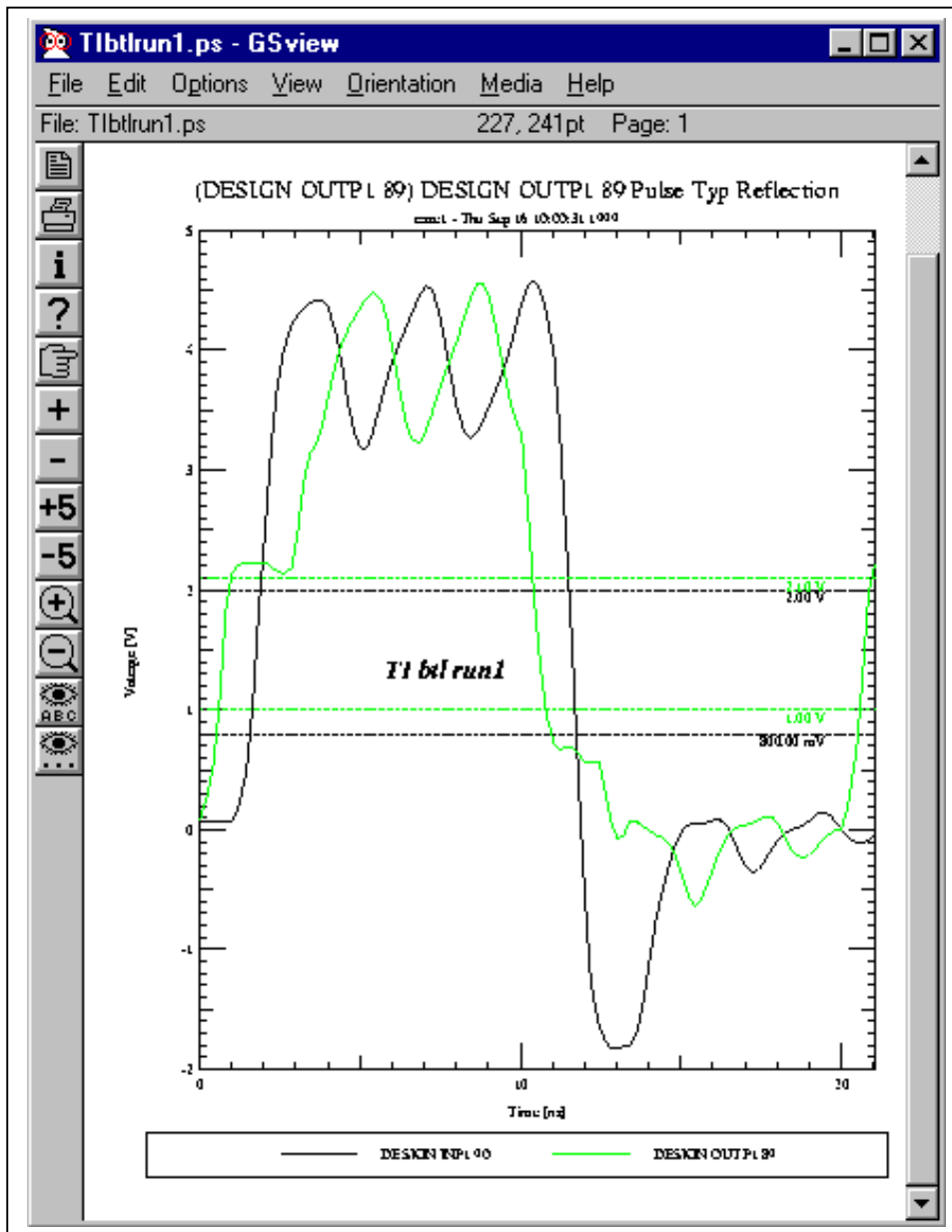
Terminated



## BTL/FB: Futurebus+ Backplane Transceiver Logic

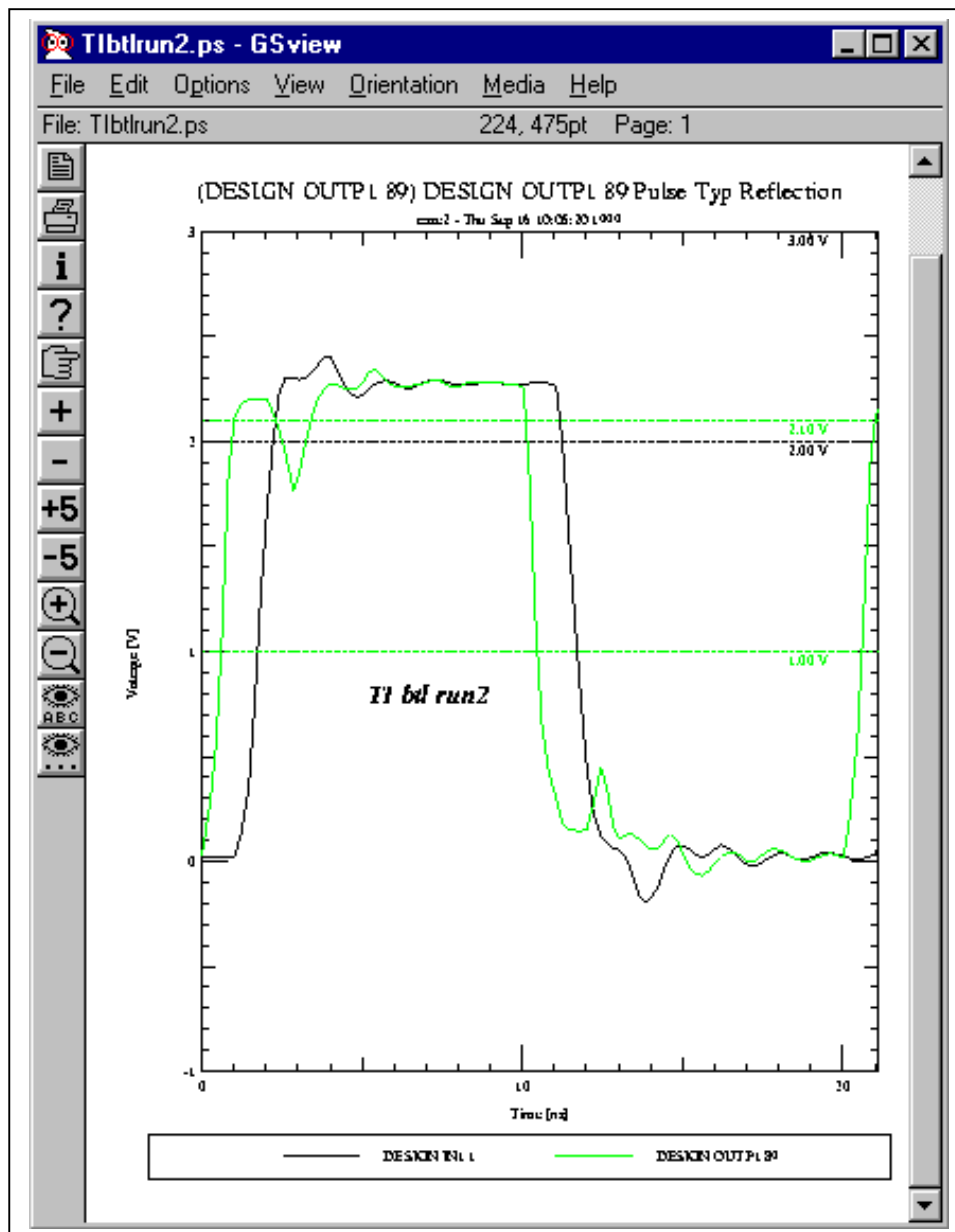
TI

Un-Terminated TTL



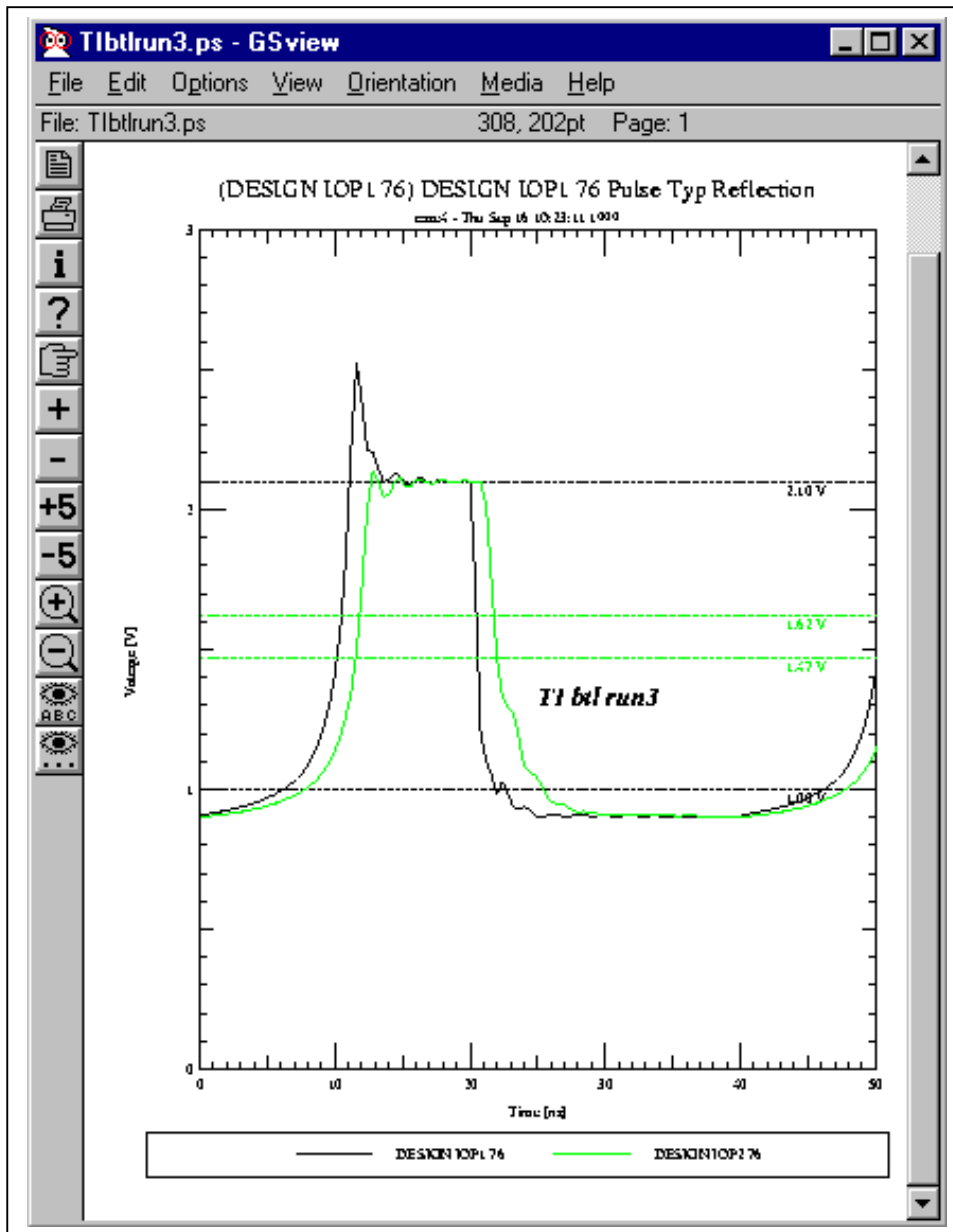
TI: Driver = FB1650\_AOUT, Receiver = FB1650\_AIN  
Run1

## Terminated TTL



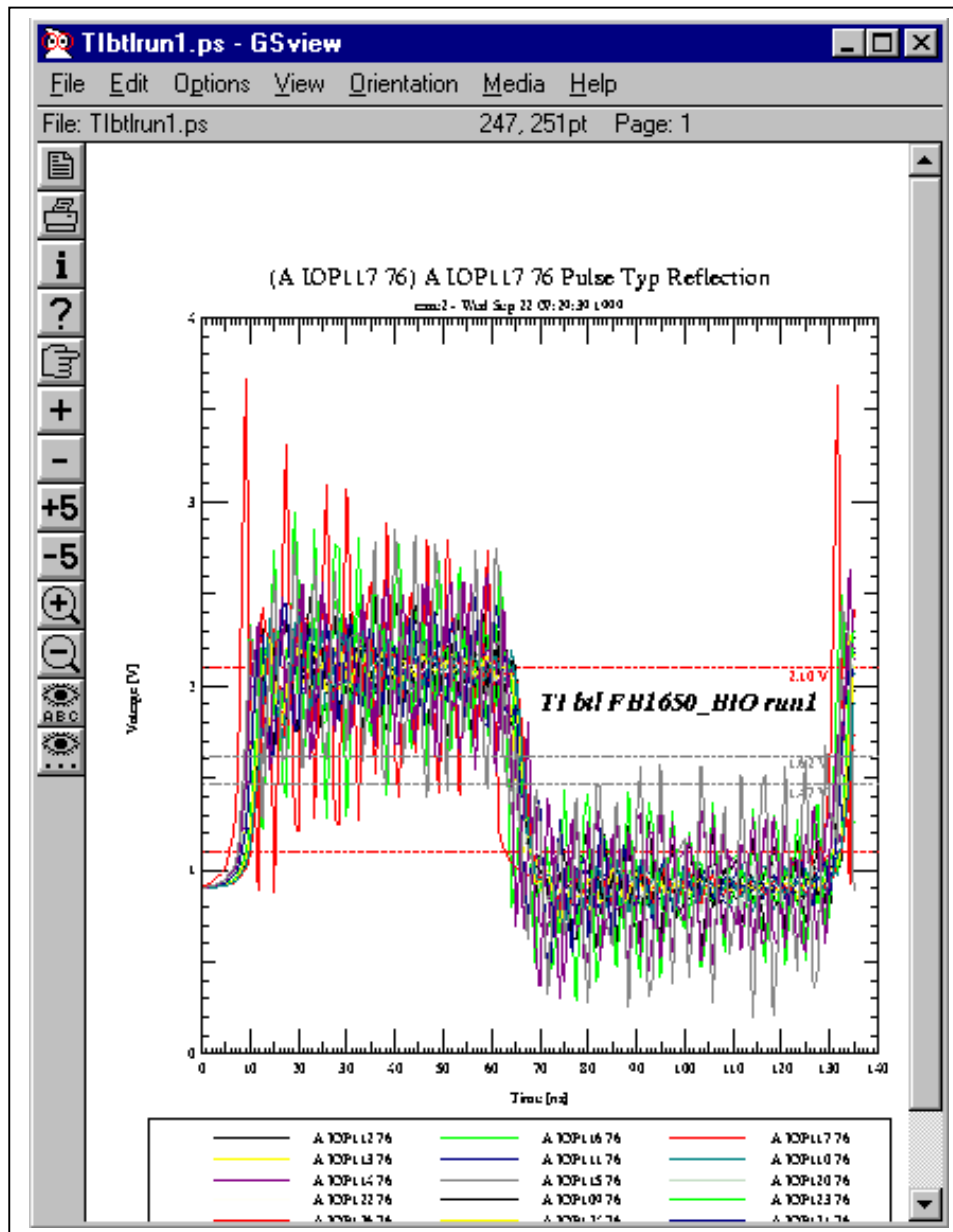
TI: Driver = FB1650\_AOUT, Receiver = FB1650\_AIN  
Run2

## BTL Point-Point



TI: Driver = FB1650\_BIO, Receiver = FB1650\_BIO  
Run3

BTL Backplane behavior. Pullup resistor at each end of backplane bus is 33 ohms,  
 $V_{pullup} = 2.1$  Volts.

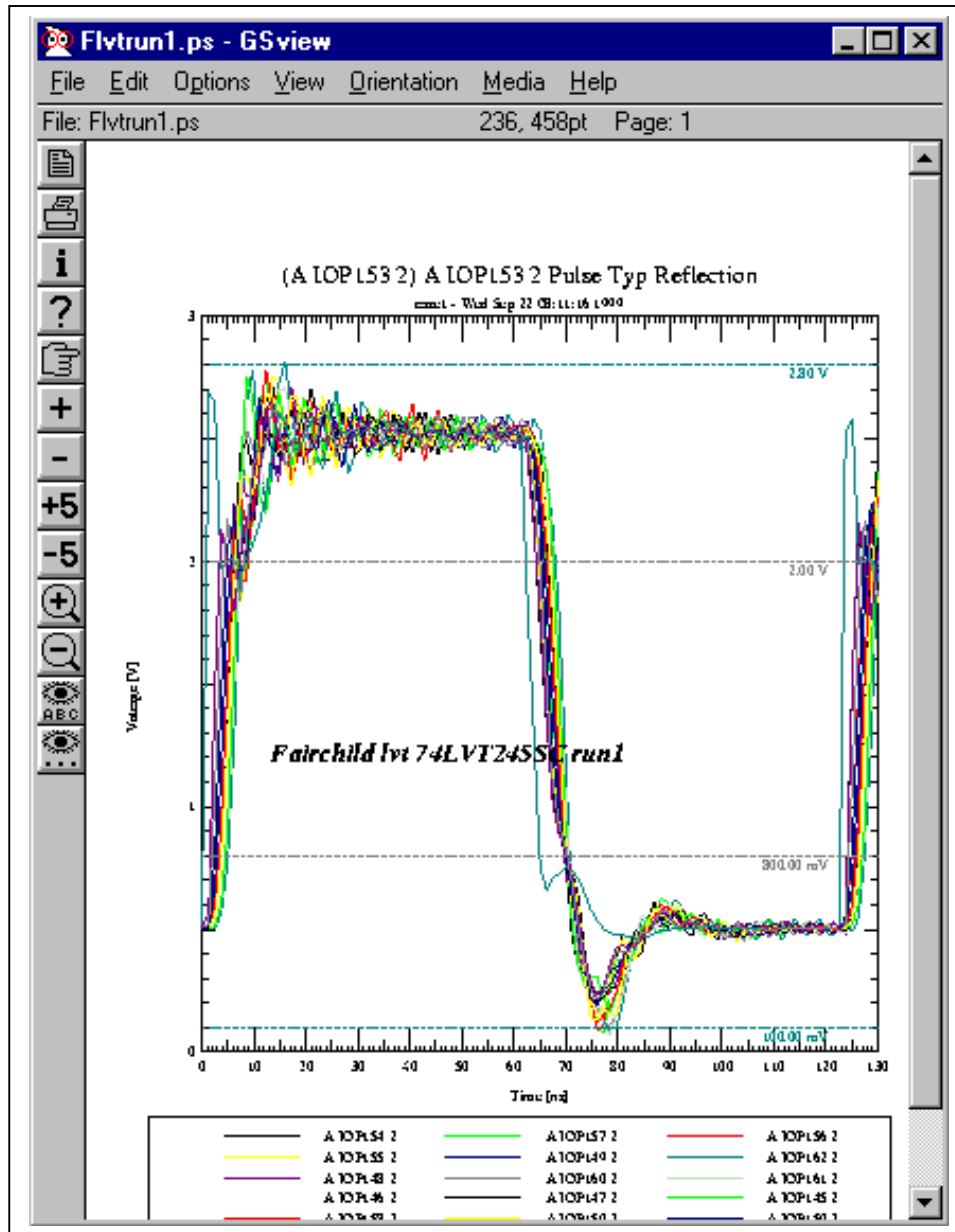


TI: Driver = FB1650\_BIO, Receiver = FB1650\_BIO  
 Run1



## LVT: Backplane Behavior

Bias network at each end of backplane bus is resistor divider of 100/75 ohms from 5 volts to ground.



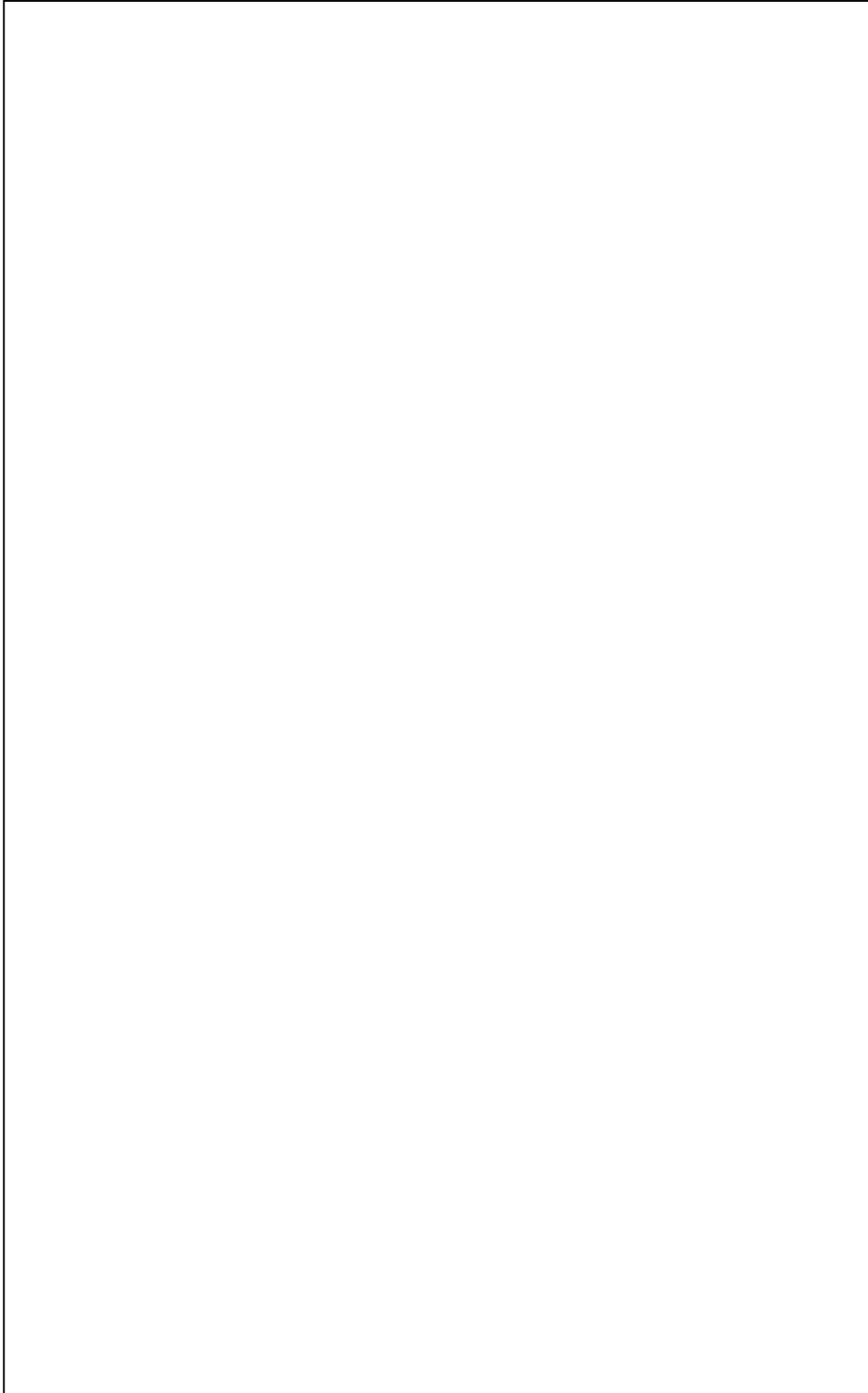
Fairchild: Driver = 74LVT245SC data\_io, Receiver = 74LVT245SC data\_io  
Run1

**\*CBT**

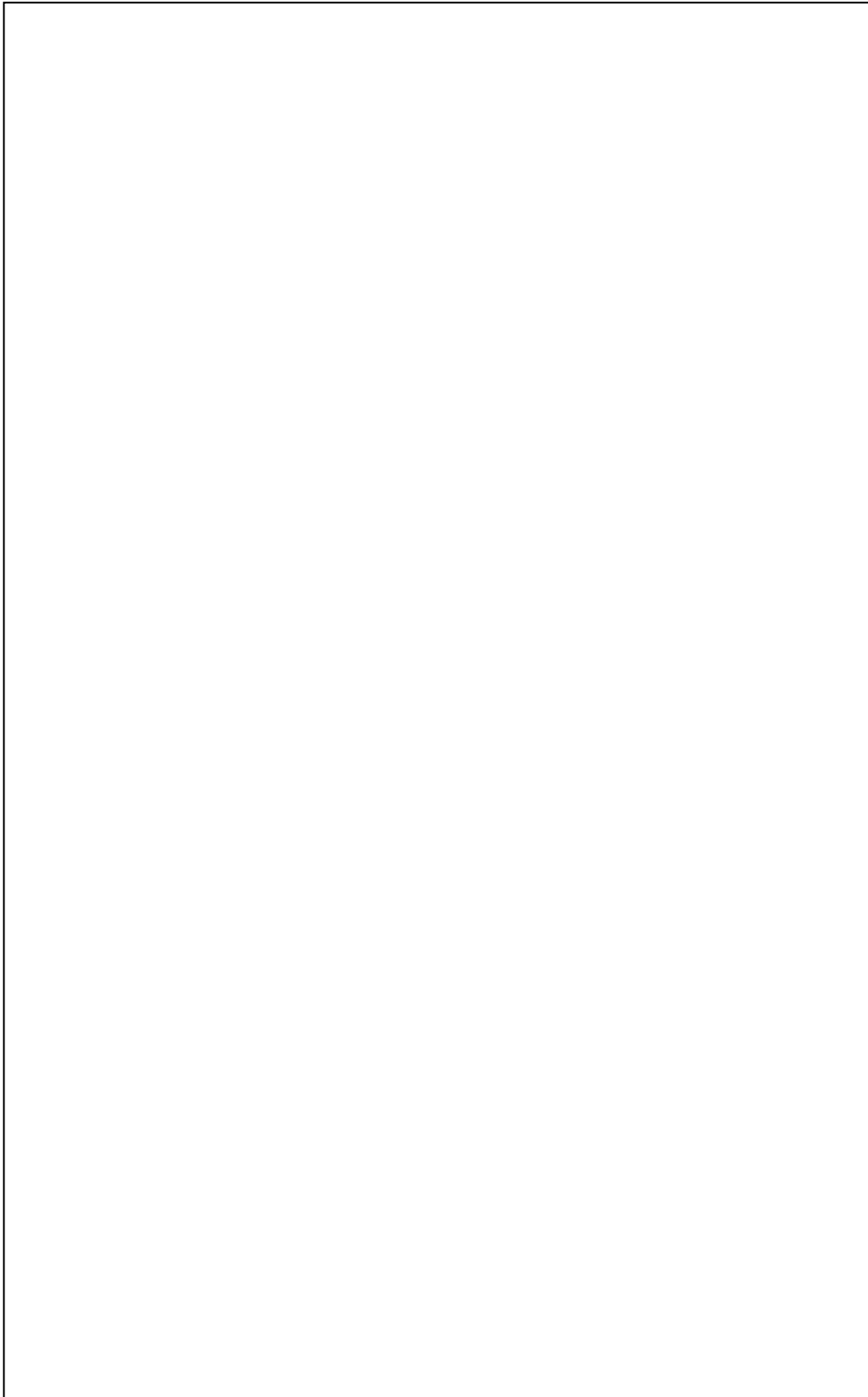
Crossbar Technology

TI

Un-Terminated



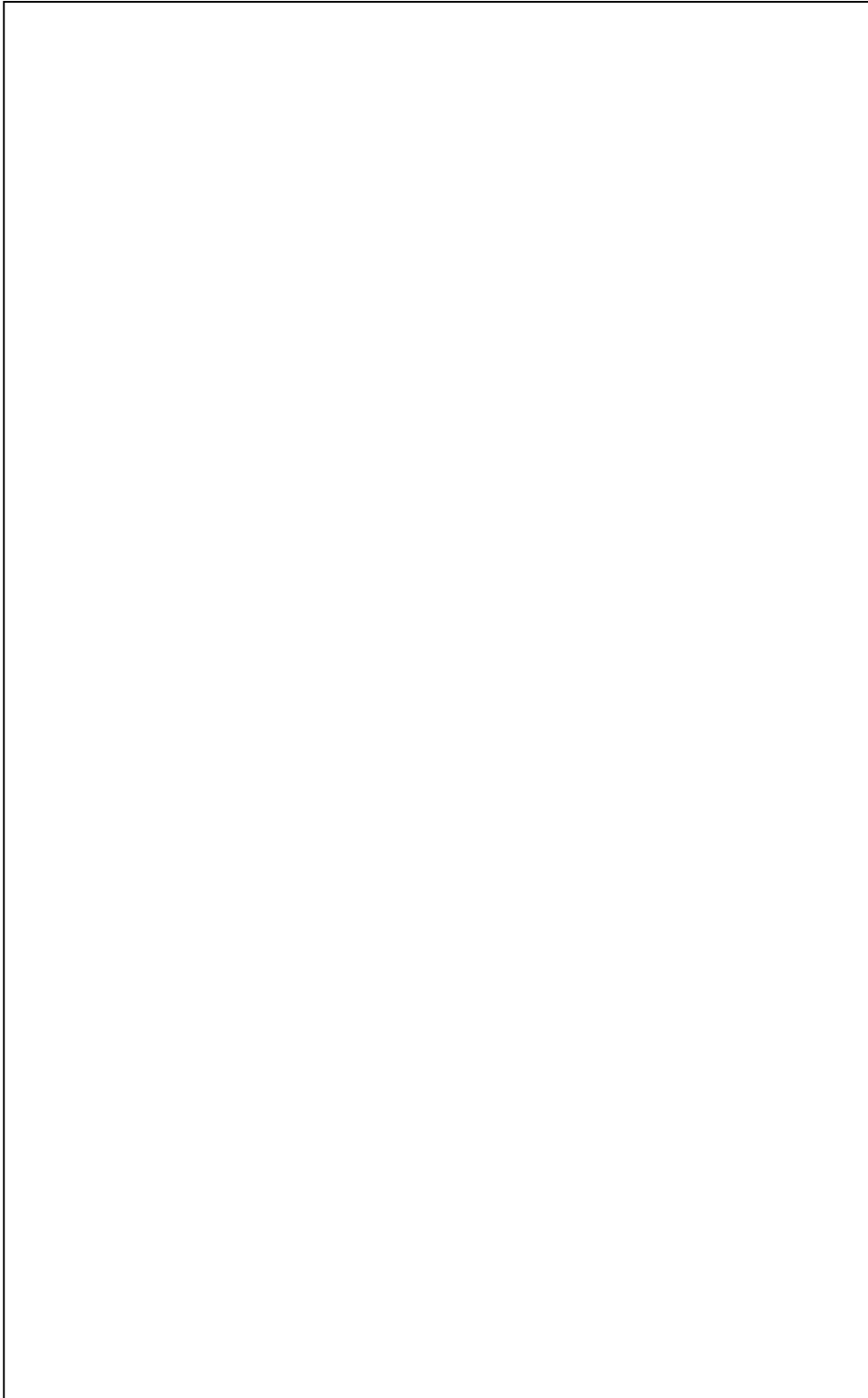
Terminated



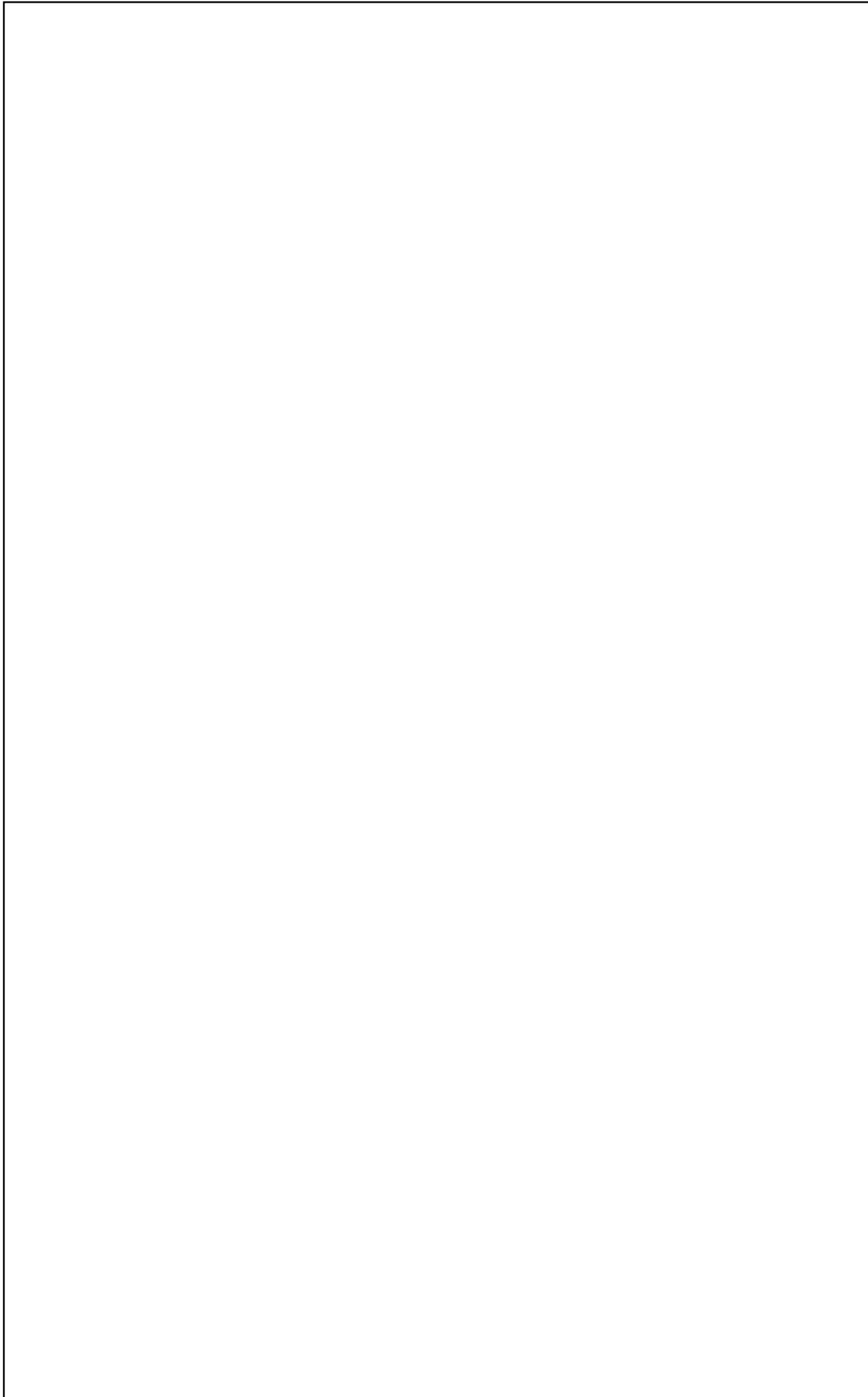
**\*CBTLV**

Low Voltage Crossbar Technology  
TI

Un-Terminated



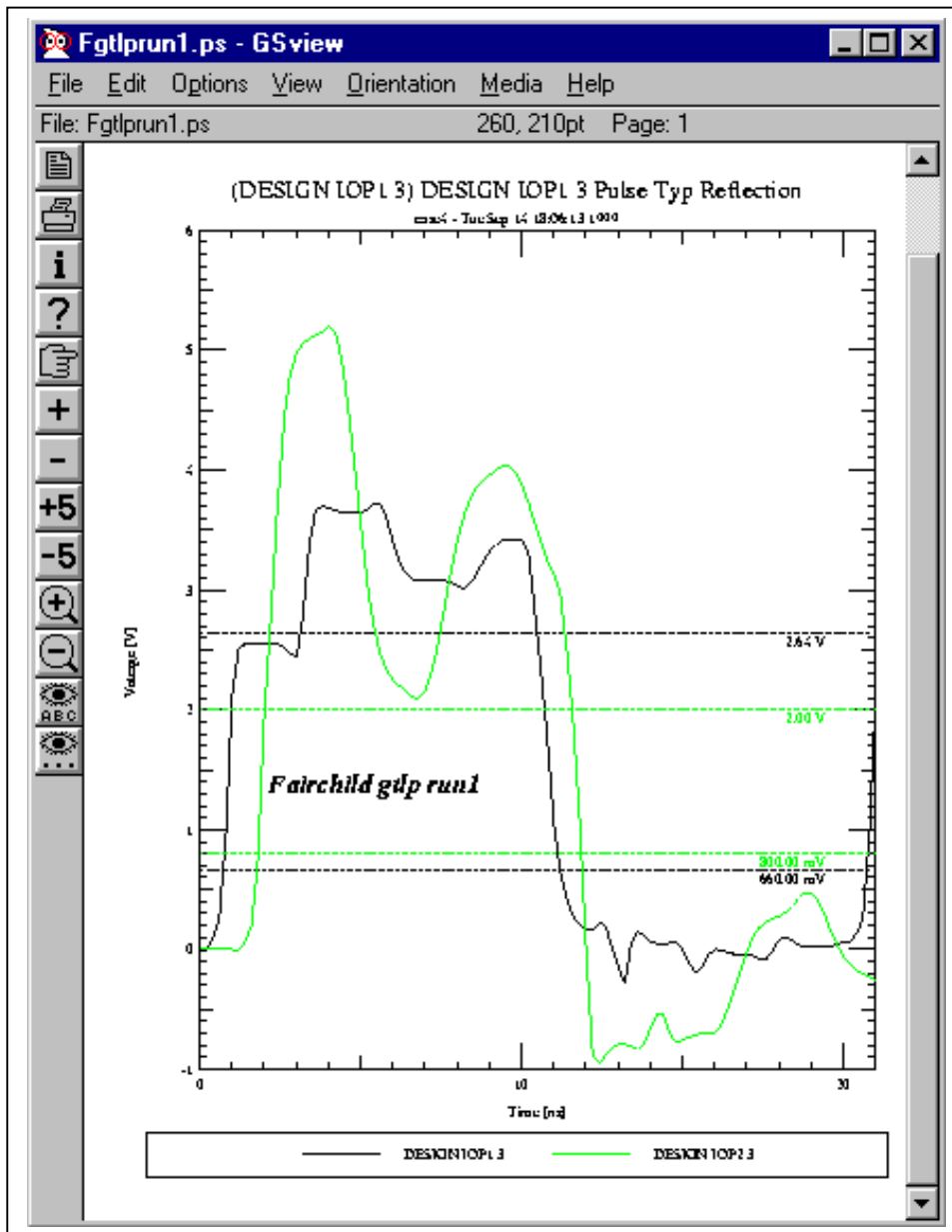
Terminated



## GTL/GTLP/GTL+: Gunning Transceiver Logic

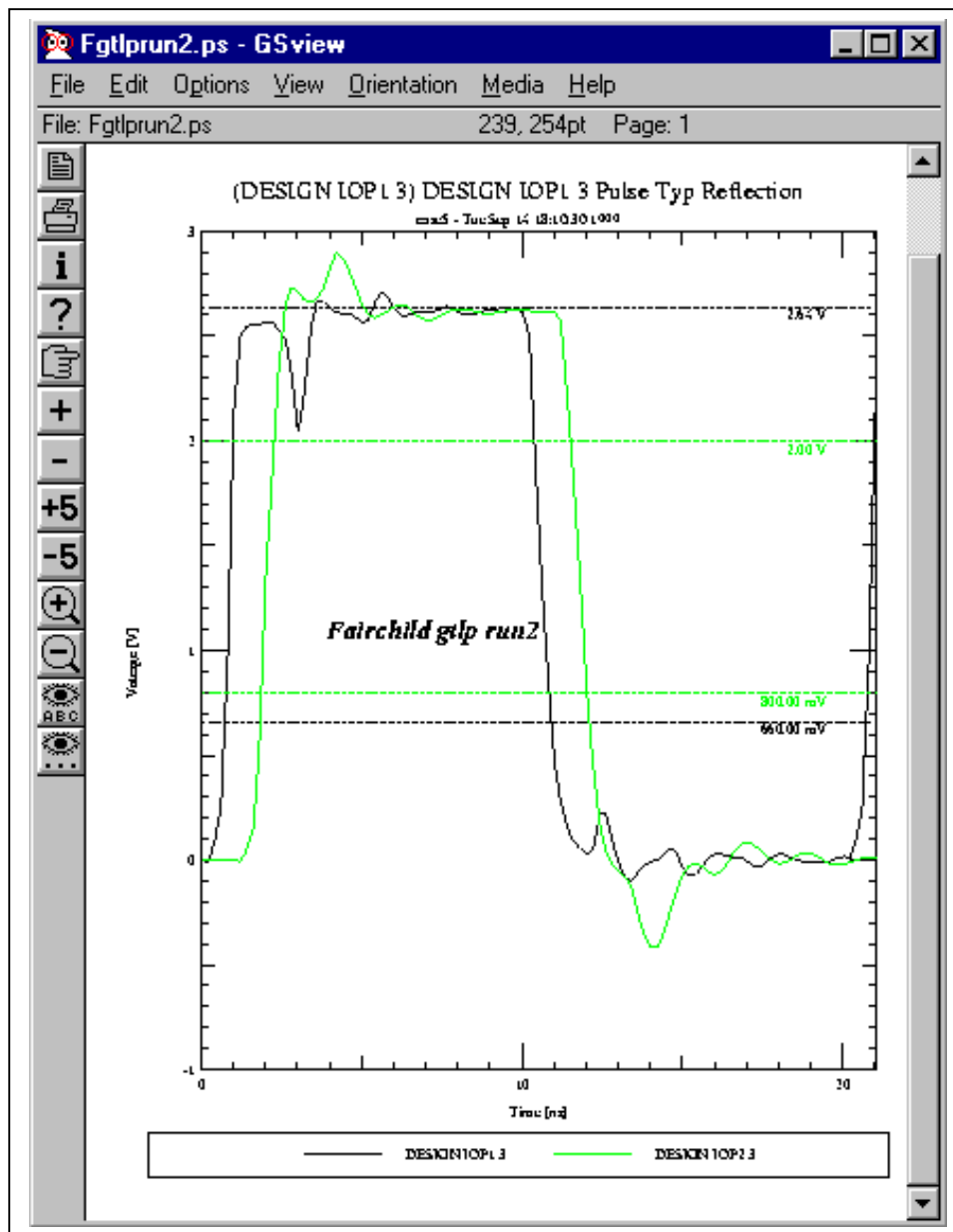
TI, Fairchild

Un-Terminated TTL



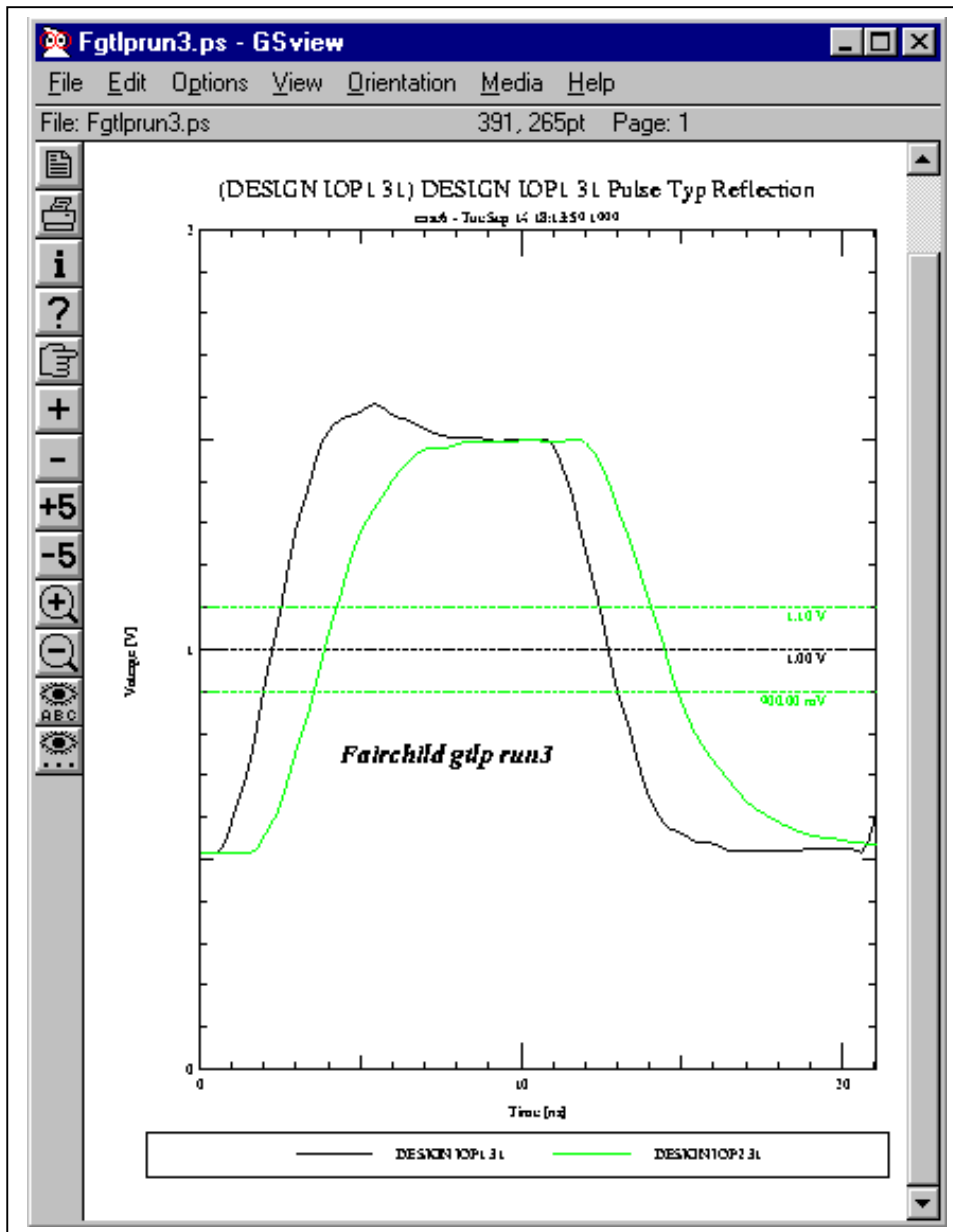
Fairchild: Driver = 74GTLP16616\_TTL (IO), Receiver = 74GTLP16616\_TTL (IO)  
Run1

## Terminated TTL



Fairchild: Driver = 74GTL16616\_TTL (IO), Receiver = 74GTL16616\_TTL (IO)  
Run2

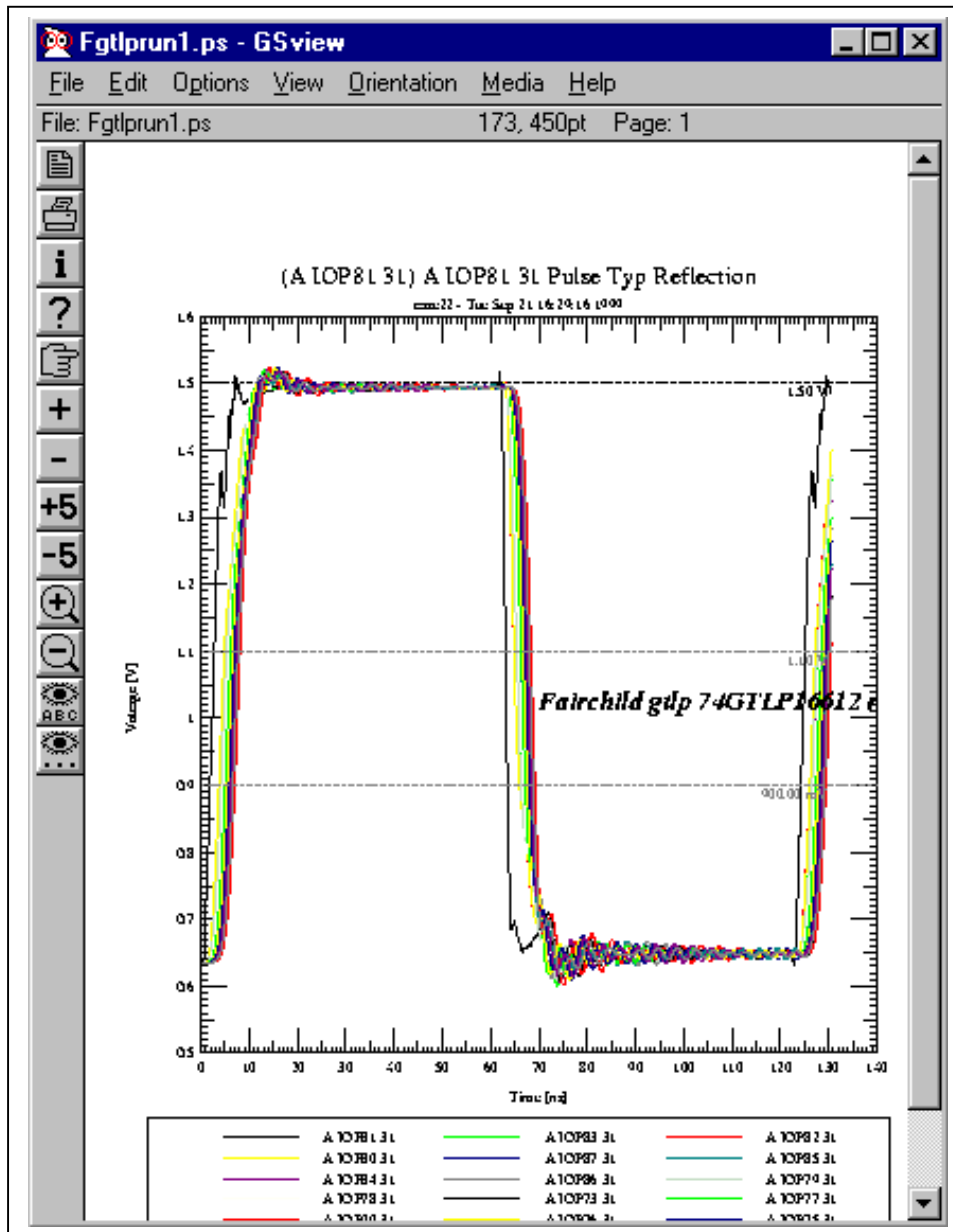
## GTLP Point-Point



Fairchild: Driver = 74GTLP16616\_GTL (IO), Receiver = 74GTLP16616\_GTL (IO)  
Run3



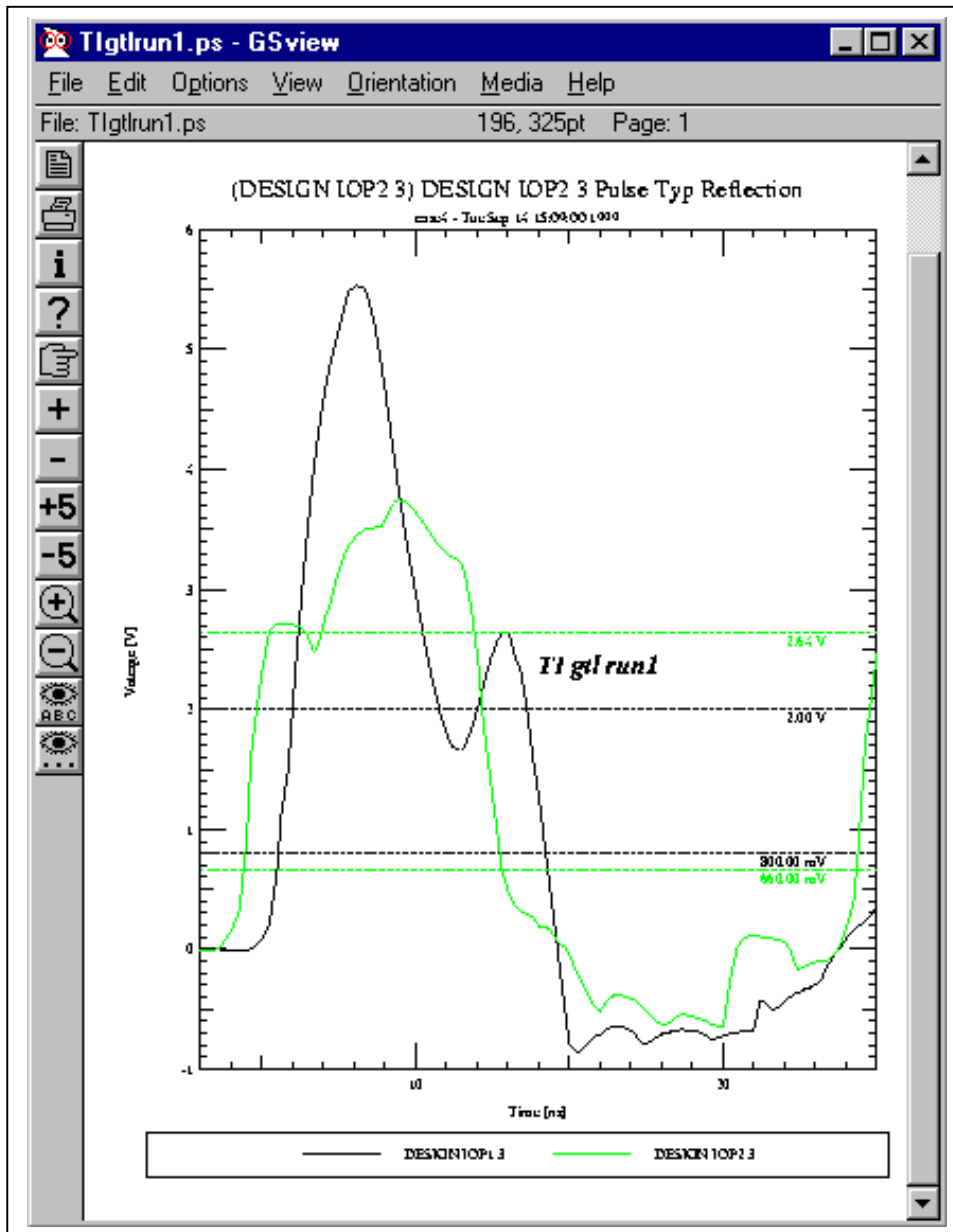
## GTLP 18 Board Backplane



Fairchild: Driver = 74GTLP16616\_GTL (IO), Receiver = 74GTLP16616\_GTL (IO)  
Run1

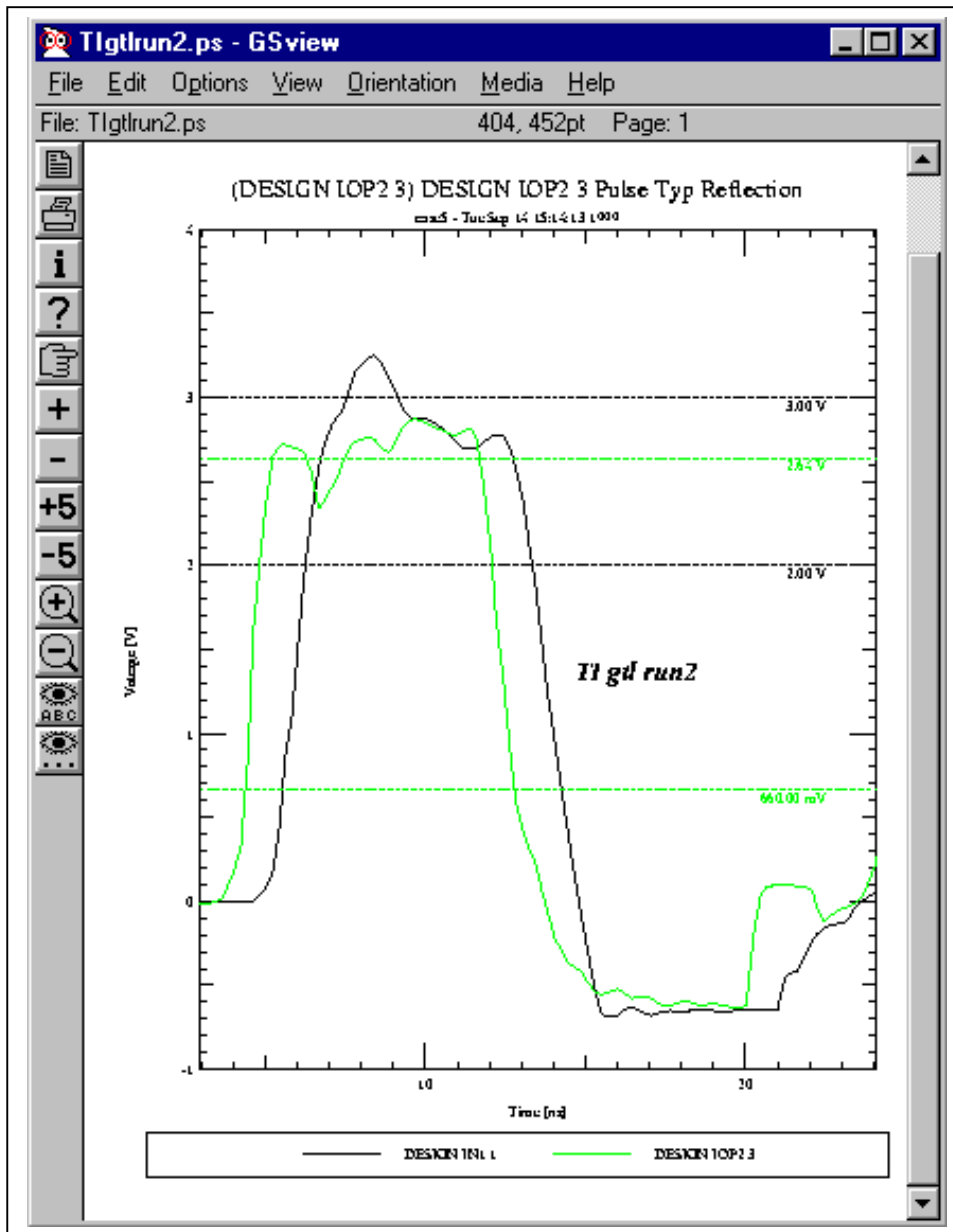
TI

TTL Un-Terminated



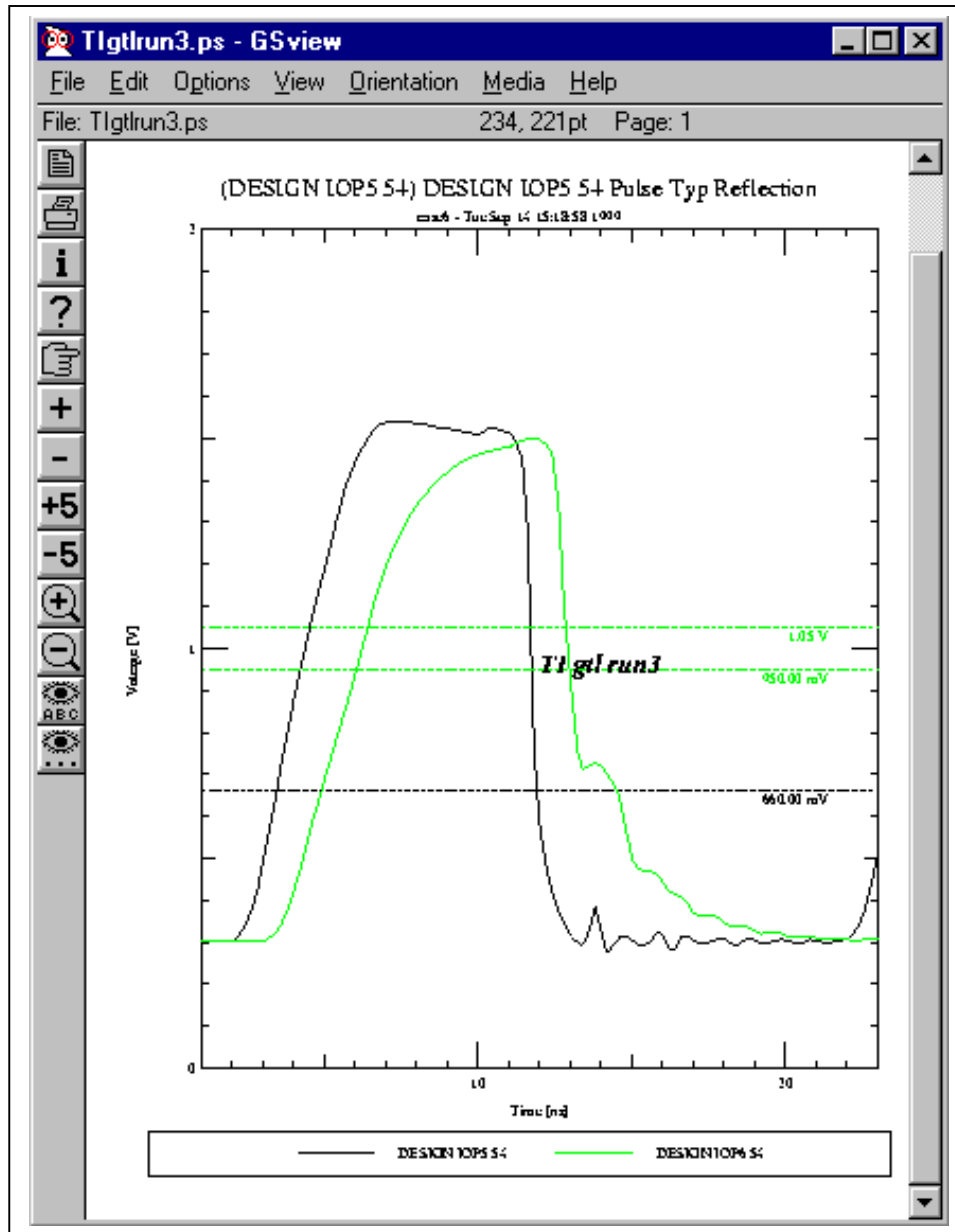
TI: Driver = 16612a\_TTL\_IO, Receiver = 16612a\_TTL\_IO  
Run1

TTL Terminated



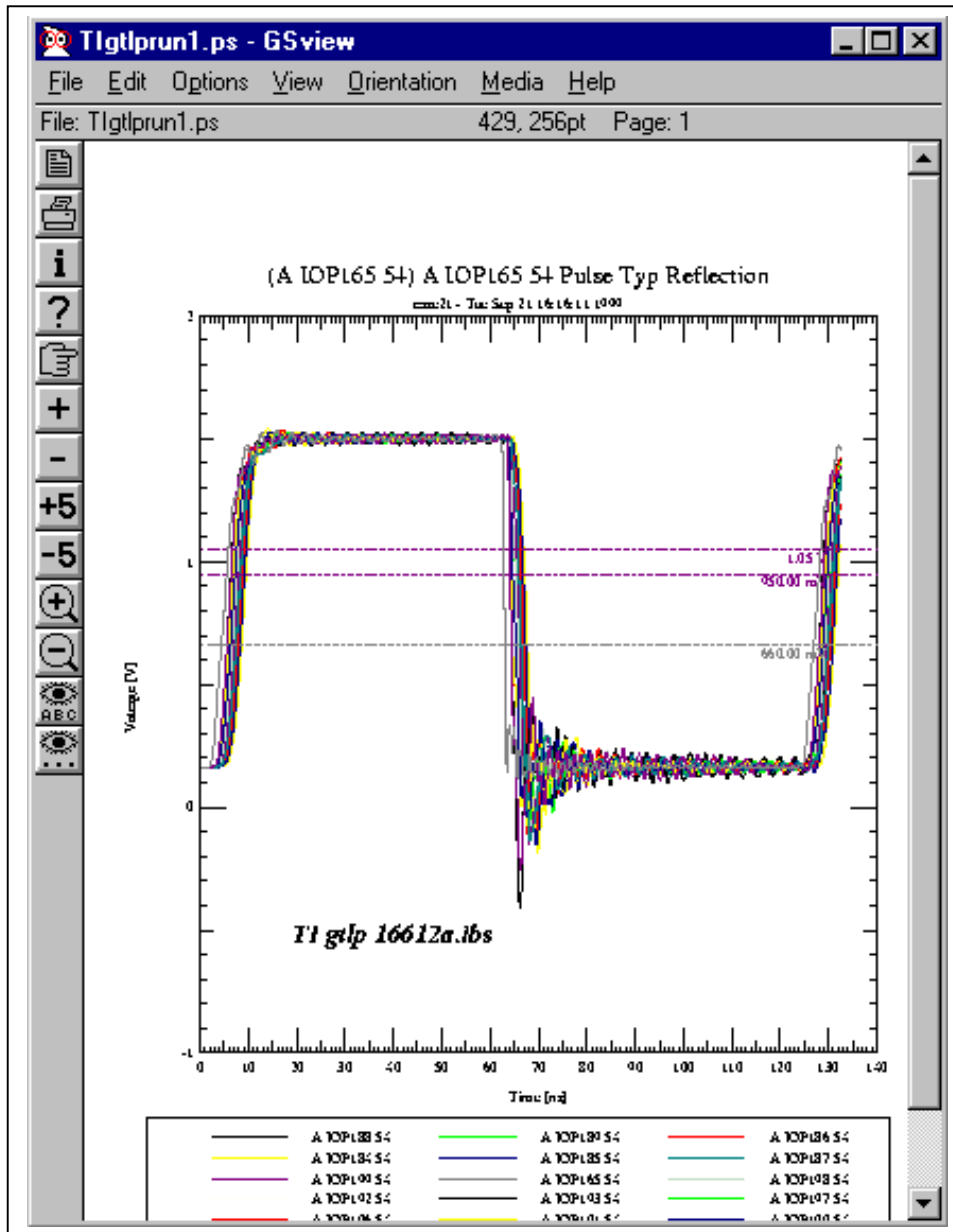
TI: Driver = 16612a\_TTL\_IO, Receiver = 16612a\_TTL\_IO  
Run2

## GTLP Point-Point



TI: Driver = 16612a\_GTL\_IO, Receiver = 16612a\_GTL\_IO  
Run3

## GTLP 18 Board Backplane



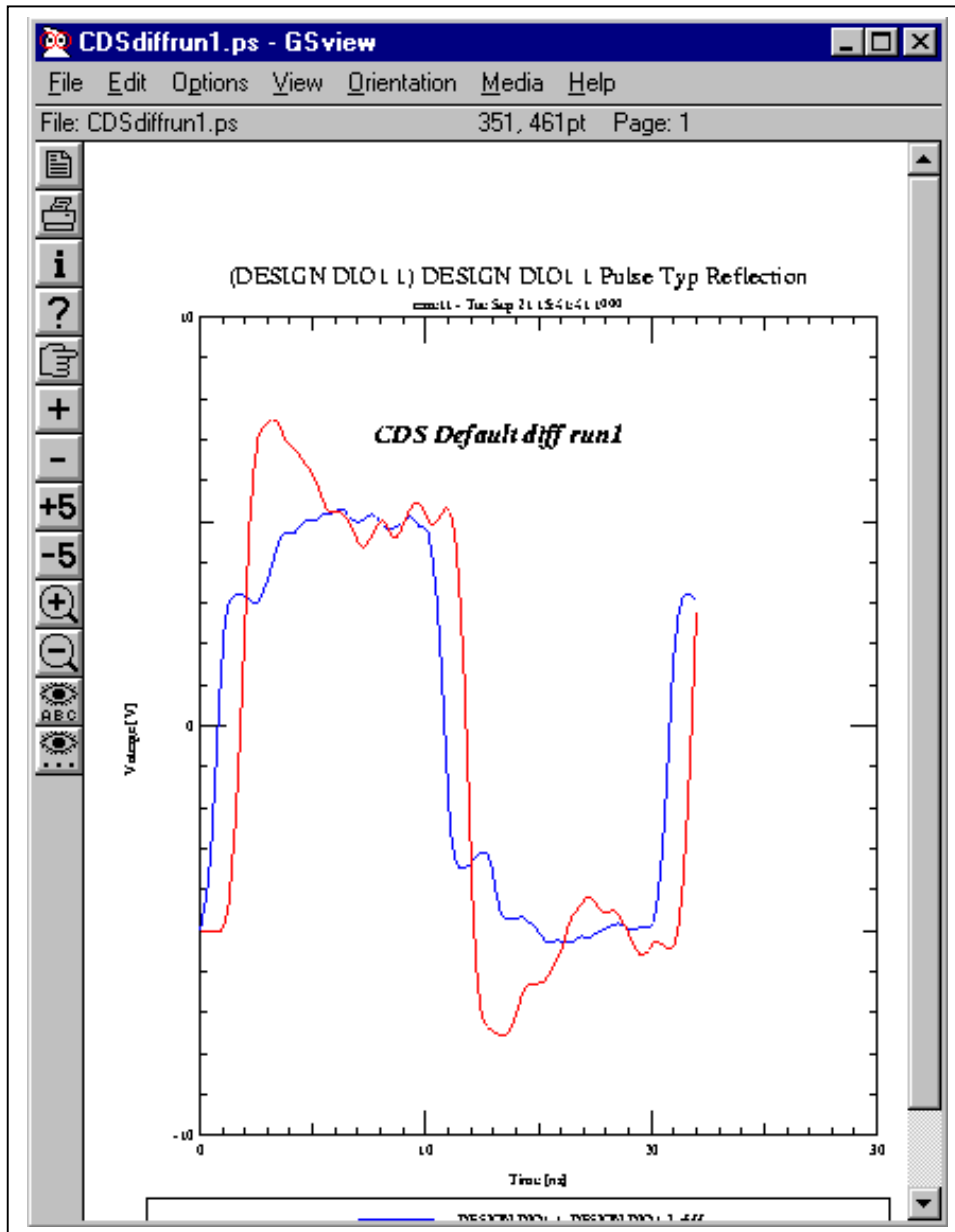
TI: Driver = 16612a\_GTL\_IO, Receiver = 16612a\_GTL\_IO  
Run1

## **Differential Nets**

CDSDefault (5 Volt), LVDS (2.5/2.1 Volt)

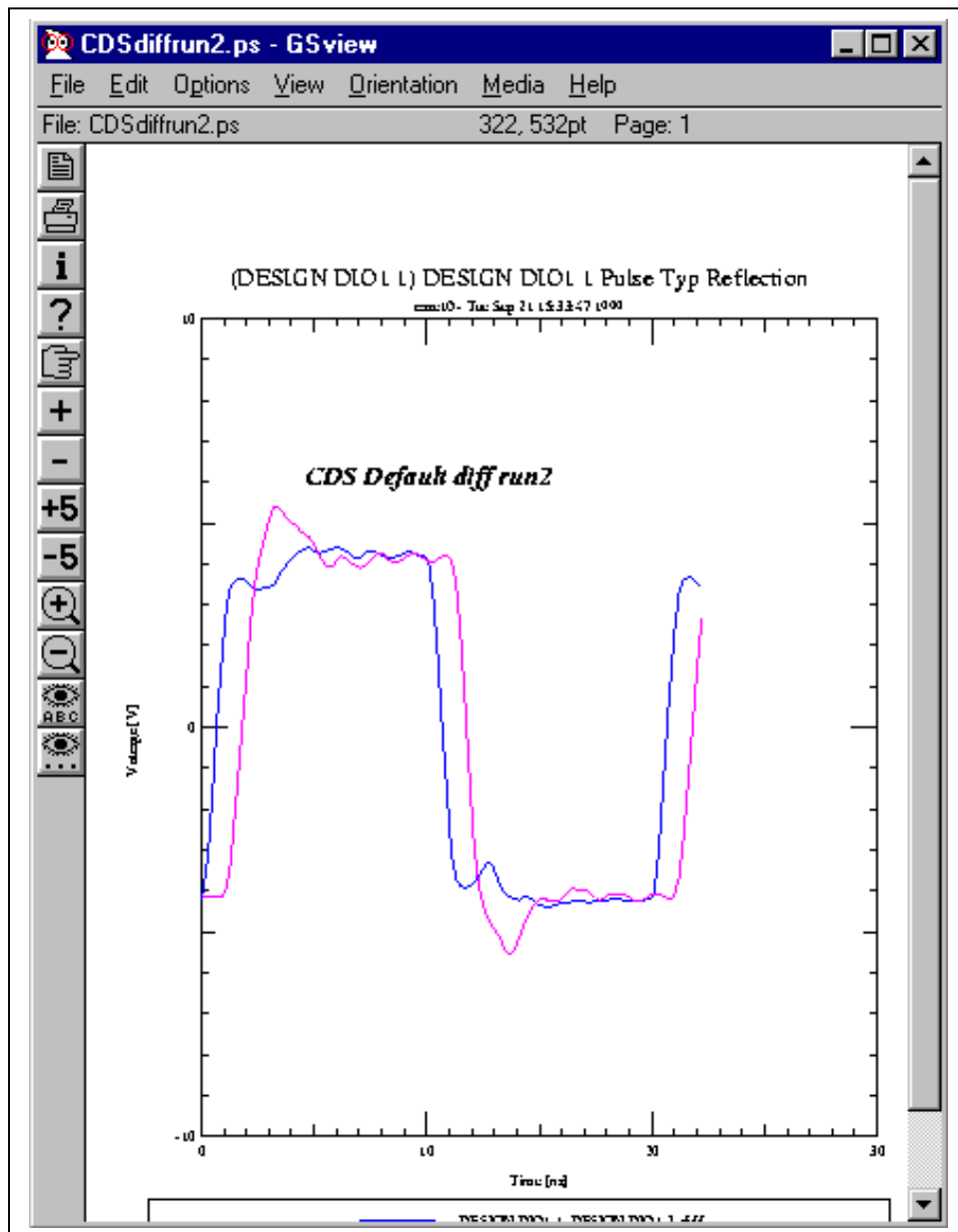
## CDS Default: Cadence Design Systems CMOS Default Differential Switch

Un-Terminated



CDS Default: Driver = CDSDefaultIO (differential), Receiver = CDSDefaultIO (differential) Run1

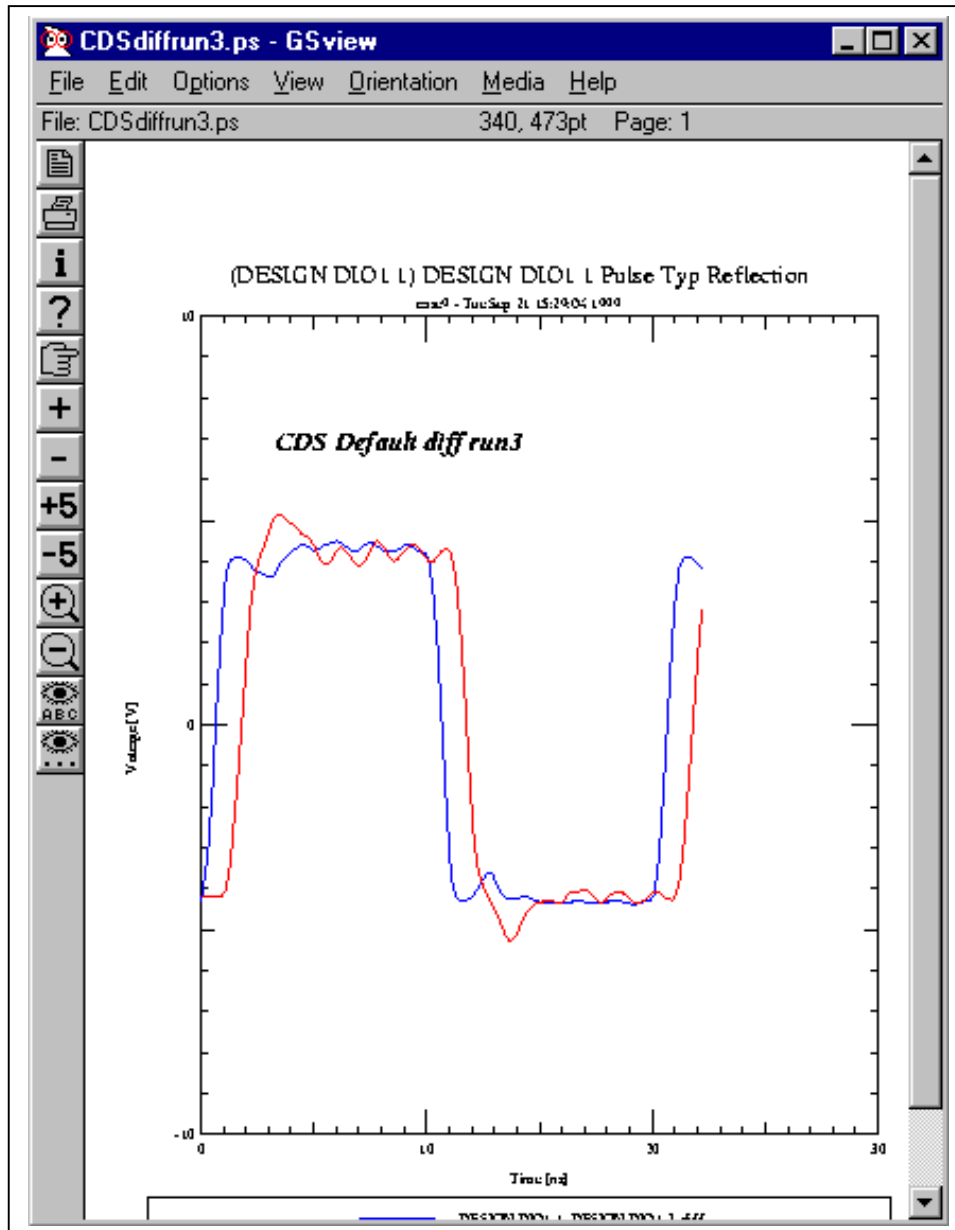
Terminated Single-Ended (78 ohms)



CDS Default: Driver = CDSDefaultIO (differential), Receiver = CDSDefaultIO (differential) Run2



Terminated Differentially (125 ohms)

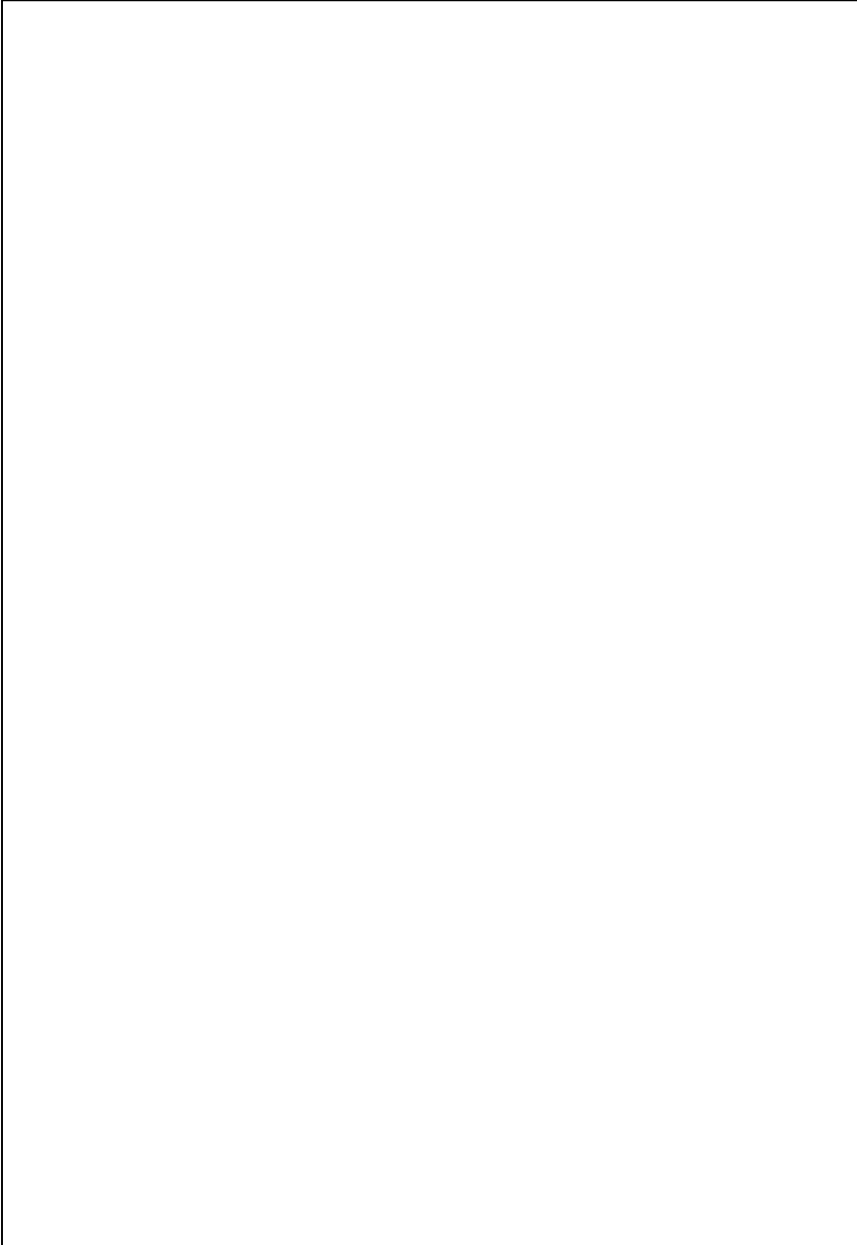


CDS Default: Driver = CDSDefaultIO (differential), Receiver = CDSDefaultIO (differential) Run3

**\*ECL: Emitter Coupled Logic**

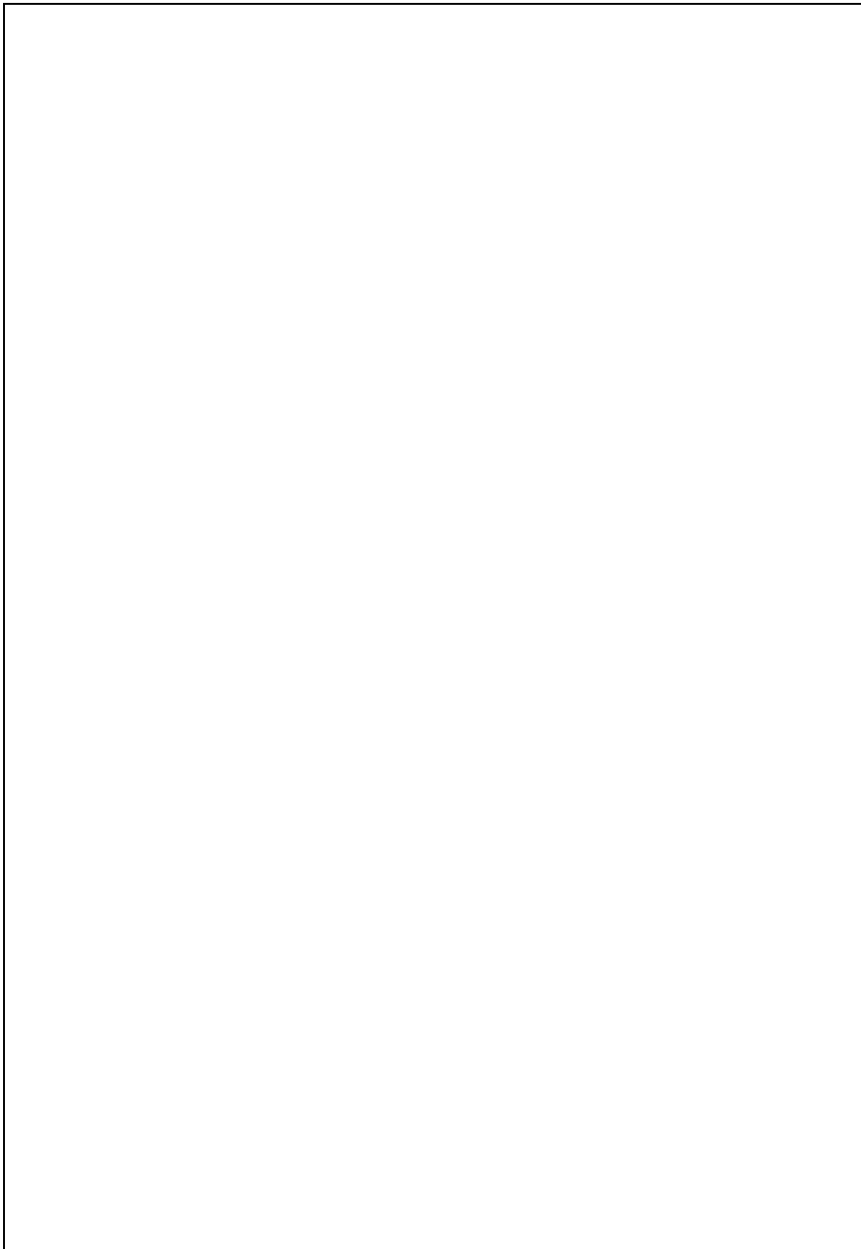
Fairchild

Unterminated



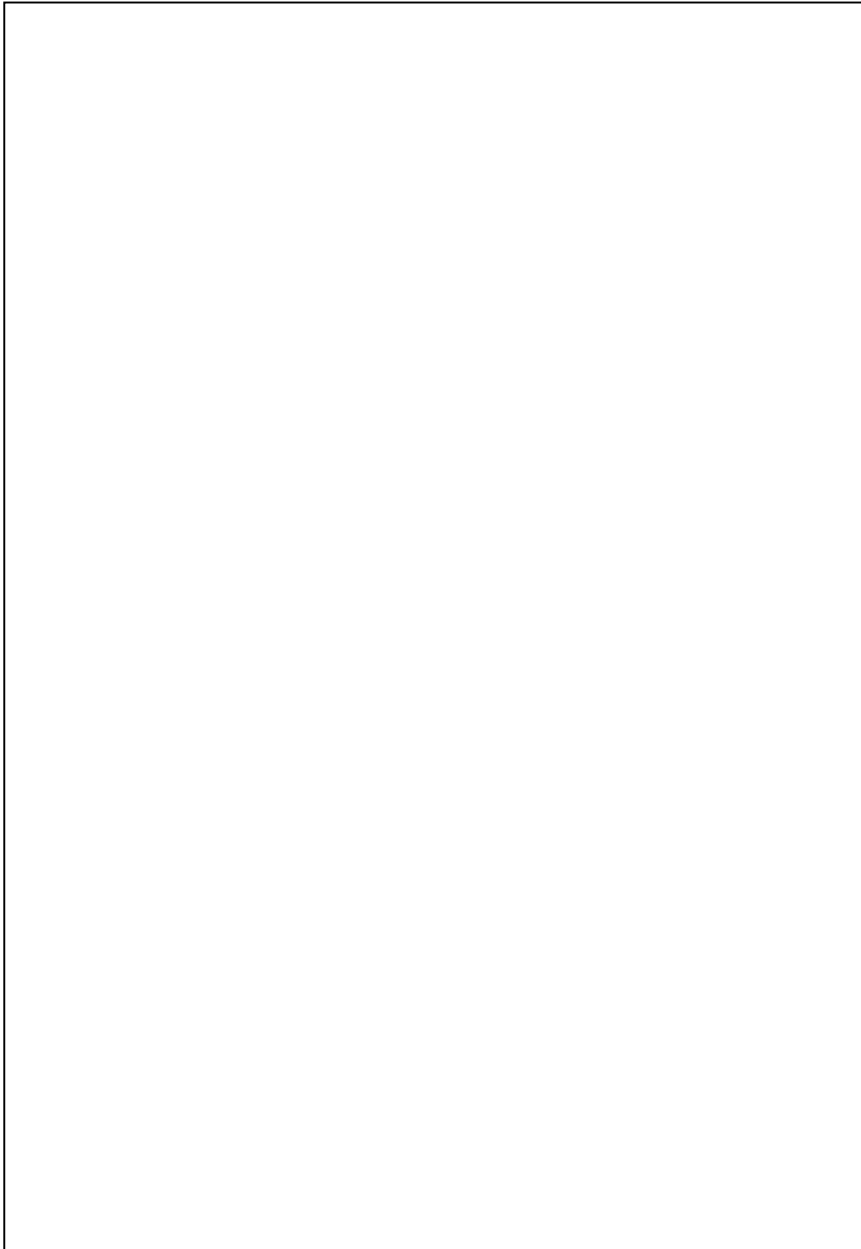
Fairchild ECL: Driver = , Receiver =  
Run1

Terminated



Fairchild ECL: Driver = , Receiver =  
Run2

Terminated

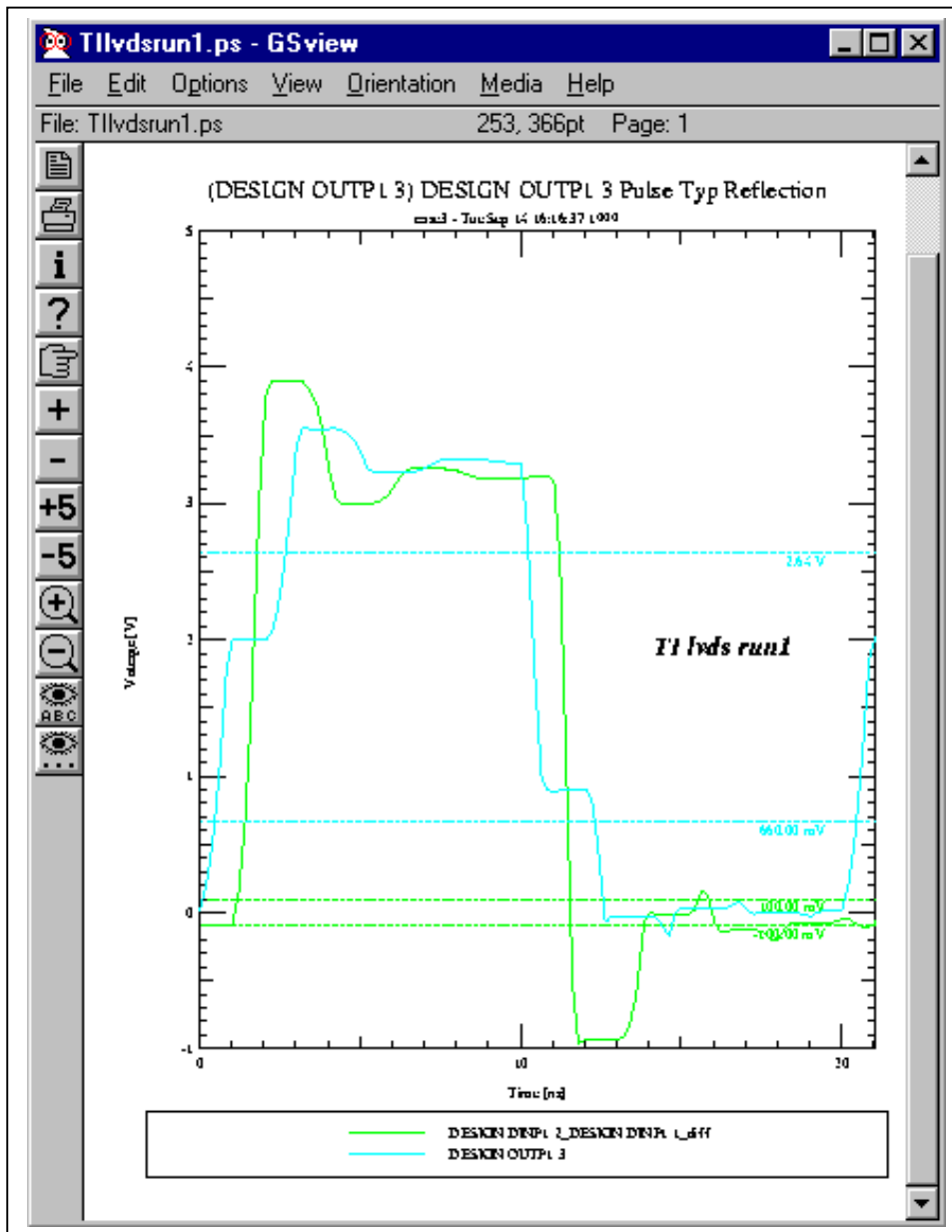


Fairchild ECL: Driver = , Receiver =  
Run3

## LVDS: Low Voltage Differential Switching

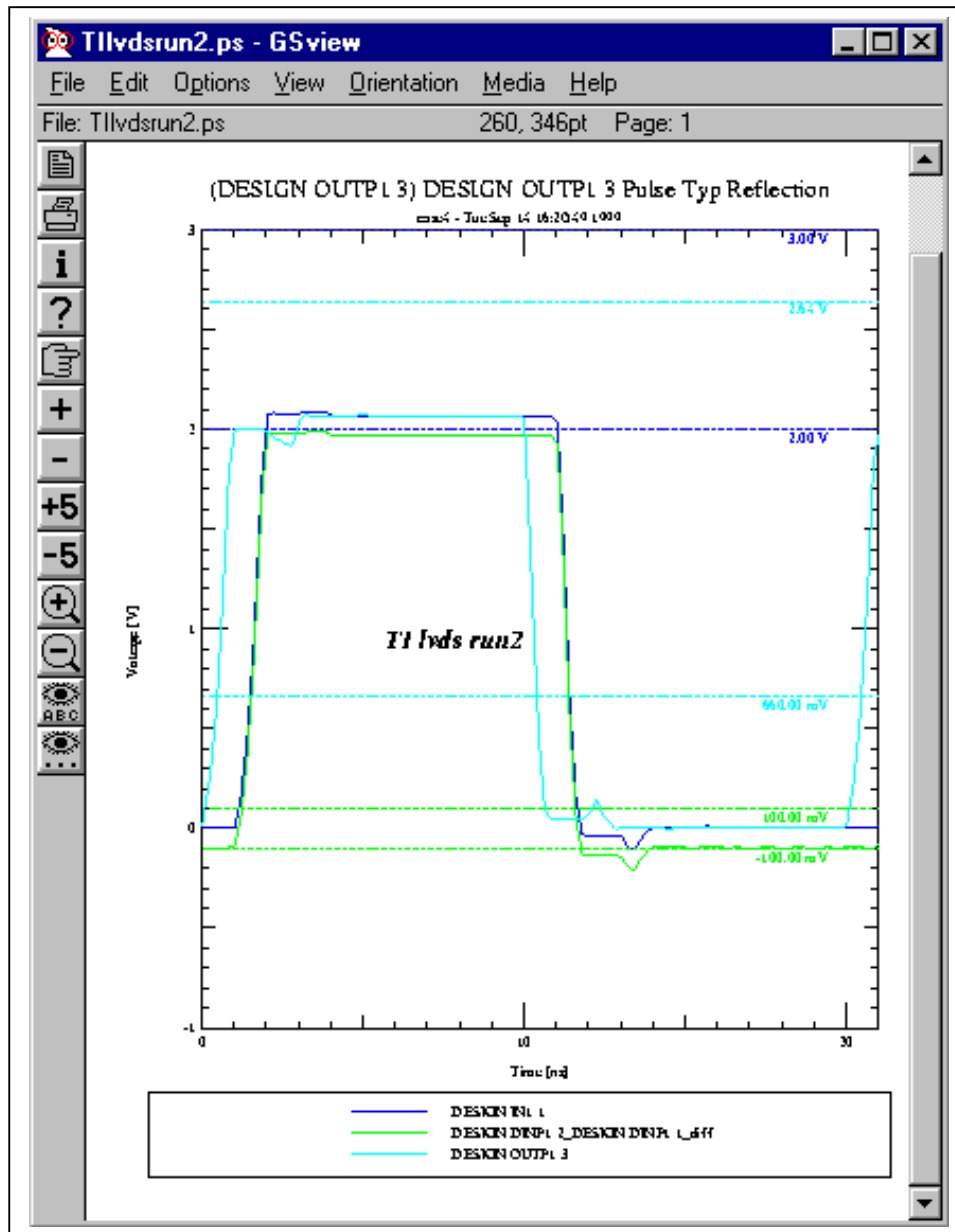
TI, NSC

Un-Terminated Single Ended



TI: Driver = SN65LVDS3486\_ROUT, Receiver = SN65LVDS3486\_RIN  
Run1

Terminated Single Ended



TI: Driver = SN65LVDS3486\_ROUT, Receiver = SN65LVDS3486\_RIN  
Run2